MG3681A
Digital Modulation Signal Generator
Contents

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Product outline

- Product outline
- Feature
- Application
- Option

- Situation
- Product concept
- Various expansion unit and software
For evaluating Base station, Mobile phone and Components for high-speed and wideband digital mobile communications systems

The digital mobile communications systems are evolved to higher speed and wider band.

» The interference to other systems of adjacent frequency band and the adjacent channel of the same system is minimized, and the modulation type with efficient transmission is adopted, in order to communicate at higher speed in the limited frequency resources.

• This signal generator that performed excellent adjacent channel leakage power ratio, wideband/high-accuracy vector modulation and various basebands is utilizable for the evaluation of high-speed digital mobile communications equipment and components in future.
For evaluating Base station, Mobile phone and Components for high-speed and wideband digital mobile communications systems

- The sensitivity (demodulation) test of base station and mobile phone receivers needs to be evaluated by wanted signal generator. Also, the receiver interference test needs to be evaluated by interference signal generator and wanted signal generator.

- Path characteristics and distortion of the components such as power amplifier, RF module and baseband need to be evaluated by signal generator and signal analyzer.
Almighty support to 3G mobile communications systems
(Product concept)

• **Excellent expansible platform**
  - Various modulation signals and AWGN are outputted by installing required expansion unit for baseband.
  - Due to the main logic circuit of expansion unit which consists of reconfigurable FPGA (Field Programmable Gate Array), users can upgrade easily by downloading the firmware including FPGA circuit data and DSP (Digital Signal Processor) program in the expansion unit.
Almighty support to 3G mobile communications systems
(Product concept)

- Successor of MG3670 series Signal Generator for second generation mobile communications systems
  - 4/5 downsizing
  - 20% cost down

MG3670 series (300k~2.75GHz)
Released in 1993, greatly contributed to the digitizing of mobile communication systems

MG3681A (250k~3GHz)
Digital and Analog modulation
30MHz wideband vector modulation

MG3641/42A (125k~2.08GHz)

High-speed data communication systems

Discover What’s Possible™
Excellent analog basic performance
(Product concept)

- **Adjacent Channel Leakage Power Ratio**
  
  In W-CDMA system, the adjacent channel leakage power ratio must be minimized in order to reduce the interference to adjacent PHS system. Extremely low adjacent channel leakage power ratio is required especially for TX power amplifier of BTS. The measurement of adjacent channel leakage power ratio of TX power amplifier requires excellent adjacent channel leakage power ratio of signal source.

  - -68 dBc/3.84MHz typ. : 5MHz offset
    - Due to Intermodulation distortion
  - -75 dBc/3.84MHz typ. : 10MHz offset
    - Due to Residual noise (Phase noise)
Excellent analog basic performance
(Product concept)

• Output level resolution
  – 0.01 dB : at all level range
Useful for fine level adjustment in components test and level calibration by power meter.

Level -143.00 dBm
Various expansion unit
The Platform with Excellent Expandability

Expansion Units is installable up to seven slots.

<table>
<thead>
<tr>
<th>Expansion Unit</th>
<th>Software</th>
</tr>
</thead>
<tbody>
<tr>
<td>MU368010A TDMA Modulation Unit</td>
<td>MX368011A PDC Software</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>MU368040A CDMA Modulation Unit</td>
<td>MX368041B W-CDMA Software</td>
</tr>
<tr>
<td></td>
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</tr>
<tr>
<td>MU368030A Universal Modulation Unit</td>
<td>MX368031A Device Test Signal Generation Software</td>
</tr>
<tr>
<td></td>
<td>MX368033A CDMA2000 1xEV-DO Signal Generation Software</td>
</tr>
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<td></td>
<td>MX368034A PDC Packet Software</td>
</tr>
<tr>
<td></td>
<td>MX368035A PHS Generation Software</td>
</tr>
<tr>
<td>MU368060A AWGN Unit</td>
<td></td>
</tr>
</tbody>
</table>

Expansion Units are internally installed.
## Expansion Unit and Software

<table>
<thead>
<tr>
<th>Communication system</th>
<th>Software</th>
<th>Expansion unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>W-CDMA / 3GPP(FDD)</td>
<td>MX368041B W-CDMA Software</td>
<td></td>
</tr>
<tr>
<td>cdmaOne</td>
<td>MX368042A IS-95 Device Test Software</td>
<td>MU368040A CDMA Modulation Unit</td>
</tr>
<tr>
<td>PDC</td>
<td>MX368011A PDC Software</td>
<td>MU368060A AWGN Unit</td>
</tr>
<tr>
<td>GSM</td>
<td>MX368012A GSM Device Test Software</td>
<td>MU368010A TDMA Modulation Unit</td>
</tr>
<tr>
<td>CDMA2000 1xEV-DO</td>
<td>MX368031A Device Test Signal Generation Software</td>
<td></td>
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<td>MX368033A CDMA2000 1xEV-DO Signal Generation Software</td>
<td></td>
</tr>
<tr>
<td>PDC Packet</td>
<td>MX368034A PDC Packet Software</td>
<td>MU368030A Universal Modulation Unit</td>
</tr>
<tr>
<td>PHS</td>
<td>MX368035A PHS Signal Generation Software</td>
<td></td>
</tr>
</tbody>
</table>

*1: Only 16QAM modulation is available in Forward, 8PSK and QPSK modulations are not available.
Neither Forward or Reverse is utilizable for receiver sensitivity test as coding format is not performed.

*2: Reverse is utilizable for receiver sensitivity test (RC1 & 3) in BS manufacturing as coding format is performed.
Forward is not utilizable for receiver sensitivity test as coding format is not performed.

*3: Continuous modulation signal based on the communication system.

The software is provided pre-installed in the expansion unit. Also, a PC memory card is provided for backup.
The software changes instantly by selecting the installed software.
At the software for the MU368030A, the signal format to output is selectable by downloading signal pattern files included in the software from a PC memory card to the waveform memory of the MU368030A Universal Modulation Unit.
MU368040A CDMA Modulation Unit

Dual output Baseband generator for Real time output and Waveform memory output

MX368041B
W-CDMA Software

MX368042A
IS-95 Device Test Software

Freq. 3000.000 000 00 MHz
Level 5.00 dBm Mem.----

Download

[Image of a Baseband generator with settings displayed on a screen: Frequency 3000.000 000 00 MHz, Level 5.00 dBm, Normal mode, System: U-CDMA, W-CDMA Phase: 0°, Simulation Link: [1.240 000 bps], Filter: [0.22], Filter Mode: TDMA, Maximum Code Number: 50, Ch. 1: On, Power: [-40.0 dB], Ch. 2: Off, Power: [-40.0 dB]]
MU368010A TDMA Modulation Unit
Baseband generator for Real time output

Download

MX368011A
PDC Software

MX368012A
GSM Device Test Software

Freq. 3000.000 000 00 MHz
Level 13.00 dBm Mem.—— Normal

Baseband: [On] [4/0 Mod.: [Int] Pulse Mod.: [Int]

System: [SS1]
Modulation: [SS]
Filter: [SS]
Differential Encode: [SS]
Burst: [SS]
Pattern: [SS]
Trigger: [SS]

Discover What’s Possible™
MU368030A Universal Modulation Unit
Baseband generator for Waveform memory output

Download

MU368030A
Universal Modulation Unit

Download

MX368031A
Device Test Signal Generation Software
MX368033A
CDMA2000 1xEV-DO Signal Generation Software
MX368034A
PDC Packet Software
MX368035A
PHS Signal Generation Software

Freq. 3000.000 000 00 MHz
Level 0.00 dBm Mem.---

Baseband : [On] [Q Mod. : [Int] Pulse Mod. : [Int]
System : [1xEV-DO]
Pattern : [MT]
Baseband Select : [Low]
Trigger Select : [Res]
Reference Clock : [Res]

Discover What's Possible™
MU368060A AWGN Unit

AWGN source for Real time output

Freq. 3000.000 000 00 00 MHz
Level 5.00 dBm Mem.

Bandwidth
System: [NOISE] Noise: [5.760MHz] Calculated: [3.840MHz]
Calculated Level: -2.19dB (Absolute): 2.81dBm
MU368040A + MX368041A + MU368060A

W-CDMA and AWGN mixing output

MU368060A

AWGN Unit

MU368040A

CDMA Modulation Unit

Download

MX368041B

W-CDMA Software

Freq. 3000,000,000,000,00 MHz

Level 5.00 dBm Mem. ---

Baseband : [On ] I/Q Mod. : [Int] Pulse Mod. : [Int]

System : [ W-CDMA ] W-CDMA Phase : [ ]

Simulation Link : [ Ctrl ] Simulation Mode : [ 3,940,000 Mbps ]

Filter : [ ] Filter Order : [ 0.22 ]


Maximum Code Number : [ ]

Ch. 1 : [On ] Power : [-40.0 dB]
Ch. 2 : [Off ] Power : [-40.0 dB]
Ch. 3 : [Off ] Power : [-40.0 dB]
Ch. 4 : [On ] Power : [-1.0 dB]
Ch. 5 : [Off ] Power : [-40.0 dB]
Ch. 6 : [Off ] Power : [-40.0 dB]
Ch. 7 : [Off ] Power : [-40.0 dB]
Ch. 8 : [Off ] Power : [-40.0 dB]
Ch. 9 : [Off ] Power : [-40.0 dB]
Ch. 10 : [Off ] Power : [-40.0 dB]
Ch. 11 : [Off ] Power : [-40.0 dB]
Ch. 12 : [Off ] Power : [-40.0 dB]

Add Ch. : [Off ] Power : [-40.0 dB]

AWGN : [On ] C/N : [-20.0 dB] Wanted : -18.5 dBm Noise : 1.5 dBm
MU368030A + MU368040A + MU368060A

CDMA2000 and AWGN mixing output

Download

MX368031A
Device Test Signal Generation Software

MX368033A
CDMA2000 1xEV-DO Signal Generation Software
# Feature

### MG3681A
- Block diagram
- Connectivity
- Excellent level accuracy signal
- Excellent signal Purity
- Phase noise
- ACLP
- Wideband and Excellent accuracy vector modulation
- Leakage emissions policy
- Operability

### Expansion unit

### Software

- Product outline
- Feature
- Application
- Option
MG3681A Block diagram

Modulation unit

14-bit

D/A

14-bit

D/A

~

I

Q

Pulse

Additional function of I/Q output (option)

I

Q

Output

Input

Vector modulator

ALC

~

AF synthesizer (option)

Input

AM

FM/φM

RF high level output (option)

Step attenuator

RF Output

AF Output

Synchronizing with Burst On/Off
Connectivity Front panel

- Display functions according to the used software and settings

- External modulation Input
  » Pulse, AM, FM, φM

- External I/Q Input
  Differential I/Q Output (Option)

- I/Q Output

- AF Output

- RF Output
Connectivity

Rear panel

- External timebase reference clock
  - 10MHz/13MHz
- PC memory card
  - PCMCIA interface
- Display functions according to the used software and settings
- GPIB remote control
- RS-232C remote control
- Trigger remote control
  - Frequency, Output level, Parameter memory (BPM number) Up/Down, RF output On/Off
Excellent level accuracy signal

For outputting with precise level

- **High-stability ALC (Automatic Level Control) circuit**
  
  Detectable at vector modulation (internal/external modulation) also
  
  » The temperature stability of ALC circuit is almost decided by temperature response of detector. The temperature response of detector has been improved by heating the detection diode with heater circuit in low temperature, which is due to the big influence of detection voltage drift especially in low temperature.

- **High-accuracy and high-reliability step attenuator**
  
  » Mechanical attenuator with excellent attenuation accuracy, small path loss and no signal distortion.
    - 1dB step, up to 140dB attenuation

- **Per-unit correction**
  
  » Frequency response, linearity error of ALC circuit and attenuation error of step attenuator are measured by the power meter and calibration receiver, then the data is inputted to correction table.
Typical level accuracy

- **Frequency response**
  
  \[ \leq \pm 0.2 \text{ dB} \]

- **Linearity**
  
  \[ \leq \pm 0.1 \text{ dB (} -127 \sim +13 \text{ dBm)} \]
Typical level stability

- **Aging**
  - CW, ALC on (default setting)
    - Almost no variation

- **Aging**
  - CW, ALC off
    - $\leq \pm 0.1$ dB
      - at ALC off
      - High-speed level switching
Typical level stability

- Aging
  - W-CDMA modulation, ALC on
  - Almost no variation (same as CW)
Typical level repeatability

- RF off → on ([on] off [on] off ...)
  - CW
  - Almost no variation

- RF off → on ([on] off [on] off ...)
  - W-CDMA modulation
  - $\leq 0.02$ dB

1st measurement level = reference(0 dB)
Typical level repeatability

- Modulation on \rightarrow\ off
  \([\text{off}^{(CW)}]\ \text{on}^{(W-CDMA)}\ \text{off}\ \text{on} \ldots\)

\[\leq 0.02\ \text{dB}\]

- Modulation off \rightarrow\ on
  \([\text{on}^{(W-CDMA)}]\ \text{off}^{(CW)}\ \text{on}\ \text{off} \ldots\)

\[\leq 0.02\ \text{dB}\]

1st measurement level = reference(0 dB)
Excellent signal Purity

Alternate adjacent channel leakage power ratio is mainly due to phase noise.

» Phase noise [dBc/Hz]

For attenuating the residual noise

• Optimization of level diagram and components
  » Circuit has been simplified to minimize the influence of non-linear components.
  » High-speed 14 bit D/A converter has been adopted, and the quantization noise leading to the residual noise has been reduced.
  » The smoothing filter which sets the cutoff frequency according to the modulation band has been passed, and out-band spurious and noise have been eliminated.
Noise of wide-band modulation signal for 3G has been lowered.

- C/N characteristic of excellent purity VCO has been applied.
  
  » Alternate adjacent channel leakage power ratio is excellent.
  
  - -145 dBc/Hz typ. : 5MHz offset
  - -150 dBc/Hz typ. : 20MHz offset
Changing Phase noise

The compression of phase noise is changed by switching the loop characteristic of PLL synthesizer circuit. Thus noise of narrow band modulation signal for 2G can be lowered also.

- PLL Mode: Normal
  The phase noise up to 100 kHz offset is improved.
- PLL Mode: Narrow
  The phase noise of 100 k to 10 MHz offset is improved.

Changing by the communication system is useful.

- W-CDMA: Normal
- CDMA2000: Narrow
- GSM/EDGE: Narrow
- PHS: Narrow
- PDC: Normal
- NADC(IS-136): Normal
Adjacent channel leakage power ratio
W-CDMA, \( \leq -3 \, \text{dBm} \) (\( \leq +5 \, \text{dBm at installing Option42} \))

Adjacent channel leakage power ratio was achieved at top level.
**Adjacent channel leakage power ratio**

**IS-95, ≤ -1 dBm (≤ +7 dBm at installing Option42)**

<table>
<thead>
<tr>
<th></th>
<th>Forward</th>
<th>Reverse</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel Count</td>
<td>9 channels</td>
<td>64 channels</td>
</tr>
<tr>
<td></td>
<td>≤ -63 dBC</td>
<td>≤ -63 dBC</td>
</tr>
<tr>
<td></td>
<td>≤ -69 dBC</td>
<td>≤ -68 dBC</td>
</tr>
<tr>
<td></td>
<td>≤ -77 dBC</td>
<td>≤ -75 dBC</td>
</tr>
<tr>
<td></td>
<td>0.885 ~ 1.25 MHz offset</td>
<td>1.25 ~ 1.98 MHz offset</td>
</tr>
<tr>
<td></td>
<td>0.885 ~ 1.25 MHz offset</td>
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</tr>
<tr>
<td></td>
<td>0.885 ~ 1.25 MHz offset</td>
<td>1.25 ~ 1.98 MHz offset</td>
</tr>
</tbody>
</table>

![Graph and Table](image-url)
**Adjacent channel leakage power ratio**

**CDMA2000 1X (RC1-2), ≤ 0 dBm (≤ +8 dBm at installing Option42)**

<table>
<thead>
<tr>
<th>Reverse</th>
<th>Forward</th>
<th>RC1 &amp; 2</th>
<th>RC3 ~ 5</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>≤ -62 dBC</td>
<td>≤ -62 dBC/30kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>≤ -67 dBC</td>
<td>≤ -70 dBC/30kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>≤ -77 dBC</td>
<td>≤ -77 dBC/30kHz</td>
</tr>
</tbody>
</table>

- ≤ -62 dBC ≤ -62 dBC/30kHz : 0.885 ~ 1.98 MHz offset
- ≤ -67 dBC ≤ -70 dBC/30kHz : 1.98 ~ 2.5 MHz offset
- ≤ -77 dBC ≤ -77 dBC/30kHz : 2.5 ~ 5 MHz offset

**CDMA2000 1X (RC3-5), ≤ -3 dBm (≤ +5 dBm at installing Option42)**

<table>
<thead>
<tr>
<th>Reverse</th>
<th>Forward</th>
<th>RC1 &amp; 3</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>≤ -62 dBC/30kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>≤ -70 dBC/30kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>≤ -77 dBC/30kHz</td>
</tr>
</tbody>
</table>

- ≤ -62 dBC ≤ -62 dBC/30kHz : 0.885 ~ 1.98 MHz offset
- ≤ -70 dBC ≤ -70 dBC/30kHz : 1.98 ~ 2.5 MHz offset
- ≤ -77 dBC ≤ -77 dBC/30kHz : 2.5 ~ 5 MHz offset
Adjacent channel leakage power ratio
CDMA2000 1xEV-DO, ≤ -3 dBm (≤ +5 dBm at installing Option42)

- ≤ -65 dBc/30kHz : 0.885 ~ 1.98 MHz offset
- ≤ -70 dBc/30kHz : 1.98 ~ 2.5 MHz offset
- ≤ -77 dBc/30kHz : 2.5 ~ 5 MHz offset
Adjacent channel leakage power ratio
PDC, $\leq +5$ dBm

**MX368011A**
- $\leq -64$ dBc/21kHz
- $\leq -68$ dBc/21kHz

**MX368031A**
- $\leq -63$ dBc/21kHz : 50 kHz offset
- $\leq -67$ dBc/21kHz : 100 kHz offset
Adjacent channel leakage power ratio
GSM/EDGE (GMSK), ≤ +5 dBm

MX368012A
- ≤ -35 dBc/30kHz
- ≤ -66 dBc/30kHz

MX368031A
≤ -35 dBc/30kHz : 200 kHz offset
≤ -66 dBc/30kHz : 400 kHz offset
Adjacent channel leakage power ratio
GSM/EDGE(8PSK), $\leq +5$ dBm

- $\leq -38$ dBc/30kHz : 200 kHz offset
- $\leq -67$ dBc/30kHz : 400 kHz offset
Adjacent channel leakage power ratio

PHS, ≤ +5 dBm

- ≤ -66 dBc/192kHz : 600 kHz offset
- ≤ -69 dBc/192kHz : 900 kHz offset
Adjacent channel leakage power ratio
NADC(IS-136), ≤ +5 dBm

- ≤ -42 dBc/24.3kHz : 30 kHz offset
- ≤ -64 dBc/24.3kHz : 60 kHz offset
- ≤ -64 dBc/24.3kHz : 90 kHz offset
Wide-band and Excellent accuracy vector modulation

The filter group according to the output frequency is switched in RF circuit to attenuate the spurious close to carrier. This filter group is the inter-digital band pass filter which can configure multi-stages in small area to satisfy out-band attenuation characteristic to eliminate the spurious in near-band, frequency response of vector modulation, pass band amplitude and group delay characteristic not to deteriorate vector modulation accuracy.

» Vector modulation frequency response (3 dB bandwidth): ≥ 30 MHz
» 3.84 Msps QPSK modulation accuracy: ≤ 2.5 % (rms)
Leakage emissions policy

The shield of signal generator is important in minimizing the signal generator’s leakage emissions which interfere to the receiver in receiver sensitivity test at low level.

» Mainframe cabinet has been structured with double shields.
» The circuit units installed in mainframe have been mounted in the shield case, respectively.
» Shield net has been equipped to display.
» PC memory card interface has been equipped to rear panel.
Operability

- **Function keys**
- **Cursor keys**
- **Color LCD**
  - Color bmp files storage
    - 640 x 480 pixel
- **Editing keys**
  - Frequency
  - Output level
  - Modulation parameters (Baseband)
    - Digital
    - Analog
  - Internal memory administration
    - Saving/Recall the setting situation
  - System setting
    - Main settings
      - Screen saver ⇒ Power-saving
      - Remote control
      - Version information
      - Operation time/count check
- **Modulation On/Off**
  - Digital
  - Analog
- **RF output On/Off**
Operability

- Panel key layout and role
  » Operability has been improved by panel layout considering smooth operation flow of [Selecting functions] → [Moving cursor] → [Editing(input/select)] → [Setting]

- Operation guidance display
  » Panel operations include the parameter settings such as item selection, data input and character input. Available key types are displayed as guidance in pop-up window during parameter setting, in order to enable the operation without confusion.
    • Example of Level Offset setting

![Example of Level Offset setting](image)

Rotary knob, Step keys, ten keys, Cursor keys
Operability

- **Modulation On/Off**
  - Digital: Vector modulation, Pulse modulation
  - Analog: AM, FM, $\phi M$
    - Internal analog modulation with AF signals of sine, triangular, square and sawtooth wave is possible at installing Option21 AF Synthesizer.
    » These modulations are switched On or Off by one touch.
    » The combination of digital modulation and analog modulation can achieve external ALC function by AM, also it is useful for the simulation of amplitude variation by AM and frequency variation by FM.
Operability

- **Internal memory administration**
  - **Basic Parameter Memory (BPM)**
    - 512 types of frequency and output level are savable.
    - Sweepable continuous recall and high-speed recall by external trigger signal are performable.
  - **All Parameter Memory (APM)**
    - all settings including the modulation parameter setting of baseband in addition to frequency and output level are savable.
    - 100 types of settings are savable regardless of the quantity of installed expansion units.
    - Max. 8 characters can be inputted each title for easy confirmation.
  - **Memory Export/Import**
    - It is useful for copying to other MG3681A and backup of memory, because BPM and APM can be save in PC memory card and recalled from PC memory card.
Expansion unit

- Expansion unit is the digital board to generate digital I/Q signal of baseband.
  - Digital I/Q signal is converted to analog I/Q signal by D/A converter.
MU368040A CDMA Modulation Unit

Block diagram

**DSP real time Generator**
- DSP
- Channel mapping
- Spreading
- Power setting

**Symbol data Generator**
- Symbol data Memory 1
- Channel mapping
- Spreading
- Power setting
- Symbol data Memory 2
- Channel mapping
- Spreading
- Power setting

**PRBS coding Generator**
- PRBS
- Channel mapping
- Spreading
- Power setting

**Arbitrary Waveform Generator**
- Waveform data Memory
- Power setting

**MU368060A AWGN Unit**
- AWGN Generator

**MU368040A Filter board**
- FIR Filter

**Add.CH**
- CH1~3 or ~4
- CH4
- CH5
- CH6~12

**I/Q**
MU368040A CDMA Modulation Unit

- **DSP real time Generator**
  - Mapping physical layer data achieved real-time coding by DSP to physical channel

- **Symbol data Generator**
  - For the channels which require power/burst control per symbol such as W-CDMA DL-DPCH and PRACH
  - Symbol signal pattern files of physical layer before spreading
    - Downloading from PC memory card to internal memory
    - Internal memory capacity
      - CH4: 4Mbit, CH5: 4Mbit
      - W-CDMA Downlink ≤ 512 ksymbol
      - W-CDMA Uplink ≤ 1 Msymbol
      - E.g. DL-DPCH 30kps: 1747 frame

- **PRBS coding Generator**
  - Mapping PRBS(Pseudo-random Binary Sequence) data to physical channel

- **Arbitrary Waveform Generator**
  - For multiple channels such as W-CDMA DPCH and OCNS
  - Signal pattern files of physical layer before FIR filtering (before over sampling)
    - W-CDMA over sampling rate: $8 \times 3.84 \text{ Mcps} = 30.72 \text{ MHz}$
    - Downloading from PC memory card to internal memory
    - Internal memory capacity
      - 512 ksamples/channel (2 Mbyte)
      - W-CDMA 3.84 Mcps ≤ 13 frame (130 ms)
MU368040A CDMA Modulation Unit

- **Firmware configuration for flexible system support**
  - Low-rate signal processor before spreading switches 2 methods according to the usage.
    - Real-time coding method by DSP
    - Memory method for downloading by cycle output of external created data pattern
  - Signal processor from high-speed spreading to FIR filtering has been adopted high accumulation FPGA of 1M gates for flexible system support.
  - These DSP programs, Signal pattern files for downloading and FPGA configuration data can be rewritten from PC memory card.
  - FIR filter which requires high-speed processing has adopted the dedicated IC, as there is not the necessity for functional change.

- **High-speed data transmission**
  - High-speed signal processing ability is required for baseband as W-CDMA specifies high-speed data communication up to 384kbps in moving state and up to 2Mbps in static state.
  - Max. 1600MIPS of high-performance DSP has been adopted for real-time coding. It enables the real-time channel coding up to 384kbps.
MU368010A TDMA Modulation Unit

Block diagram

\[ \pi /4DQPSK \text{ (PDC)} \]

- DSP
- Frame coding
- IQ mapping
- FIR Filter

\[ \text{GMSK (GSM)} \]

- DSP
- Frame coding
- Gaussian filter
- MSK

I/Q
**MU368030A Universal Modulation Unit**  
Block diagram

- **Arbitrary Waveform Generator**
  - Signal pattern files after filtering
    - Downloading from PC memory card to internal memory
      - Internal memory capacity 16 Msamples/channel (64 Mbyte)
      - Sampling rate $\leq$ 20 MHz
Software

• MX368041B  W-CDMA Software  54
  – MX368041B-11  HSDPA Signal Pattern  56
  – MX368141A  HSDPA IQ producer  73
• MX368042A  IS-95 Device Test Software  77
• MX368011A  PDC Software  84
• MX368012A  GSM Device Test Software  92
• MX368031A  Device Test Signal Generation Software  102
• MX368033A  CDMA2000 1xEV-DO Signal Generation Software  111
  » MX368133A  CDMA2000 1xEV-DO IQproducer™  120
• MX368034A  PDC Packet Software  126
• MX368035A  PHS Signal Generation Software  133
• MU368060A  AWGN  141
MX368041B W-CDMA Software

- Downlink/Uplink W-CDMA test signals for 3GPP(FDD) standard can be outputted by installing the MX368041B W-CDMA Software in the MU368040A CDMA Modulation Unit.
- In R&D/production process of components, base stations (BS) and user equipment (UE), the functions to support various applications are provided as the signal source for components, the wanted signal source and the interfering signal source for receiver test.
Support of test signal format

- Just to select the signal patterns for TS 25.141 and TS 34.121 test specifications without setting complicated parameters of 3GPP!

  **Simple operation**

- Quick support is provided by updating the signal pattern files saved from PC memory card to internal memory and DSP program for real-time coding.

  » Supporting 3GPP update and special signal patterns
    - “Product Introduction MX368041A/B Update News” is provided.
      Version-up History, How to check Version, How to upgrade, File configuration in PC memory card, Signal pattern List

Selecting Signal pattern in internal memory

Confirming of Signal pattern contents
This package added the signal pattern file specified in Release 5 to Release 1999 signal pattern file of an appendix in MX368041B.
## Signal patterns

For evaluating components in BS transmitter

<table>
<thead>
<tr>
<th>Test Item</th>
<th>Channel combination</th>
<th>Parameter</th>
<th>Patt. name</th>
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<td>TS25.141 6.1.1</td>
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<td>B11657d</td>
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<td>B11657d2</td>
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<td>32 DPCH</td>
<td>BS13257</td>
<td>B13257d</td>
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<td>BS132571</td>
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<td>64 DPCH</td>
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<td>BS164571</td>
<td>B16457d2</td>
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<td>TS25.141 6.1.1.3</td>
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<td>16 DPCH</td>
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<td>Test Model 3</td>
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<td>BS316571</td>
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<td>32 DPCH</td>
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<td>TS25.141 6.1.1.4</td>
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</tr>
<tr>
<td>TS25.141 6.1.1.4A</td>
<td>TS25.141 6.1.1.4A</td>
<td>2 HS-PDSCH + 6 DPCH</td>
<td>BS5_257</td>
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<tr>
<td>Test Model 5</td>
<td></td>
<td></td>
<td>BS5_2571</td>
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<td>BS5_2572</td>
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</tr>
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<td></td>
<td></td>
<td>BS5_2573</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>4 HS-PDSCH + 14 DPCH</td>
<td>BS5_457</td>
<td></td>
</tr>
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<td>BS5_4571</td>
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<td></td>
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<td>BS5_4573</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>8 HS-PDSCH + 30 DPCH</td>
<td>BS5_857</td>
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<td>BS5_8571</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>BS5_8573</td>
<td></td>
</tr>
</tbody>
</table>

2 carriers

- 6.1.1.1
  Test Model 1 Multi-carrier (2 carriers)

- 6.1.1.4A
  Test Model 5 (HSDPA)
  - Multi-carrier (2 carriers)

****d: for lower freq.
****d2: for higher freq.
### Signal patterns

For receiver and performance testing for BS

<table>
<thead>
<tr>
<th>Test Item</th>
<th>Channel combination</th>
<th>Parameter</th>
<th>Patt. name</th>
<th>Added by option 11</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 Receiver characteristics</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8 Performance requirement</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8.8.1 RACH preamble</td>
<td>TS25.211 5.2.2.1</td>
<td>TS25.213 4.3.3</td>
<td>PRE</td>
<td></td>
</tr>
<tr>
<td>8.9.3 CPCH message</td>
<td>TS25.211 5.2.2.2</td>
<td>TS25.141 Annex A8</td>
<td>C168  C360</td>
<td></td>
</tr>
<tr>
<td>8.10 SSDT</td>
<td>TS25.141 Annex A1</td>
<td>TS25.141 Annex A2</td>
<td>SSDTa  SSDTb</td>
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</tbody>
</table>

- **8.8 RACH performance**
  - 8.8.1 RACH preamble detection in static propagation conditions
  - 8.8.2 RACH preamble detection in multipath fading case 3
  - 8.8.3 Demodulation of RACH message in static propagation conditions
  - 8.8.4 Demodulation of RACH message in multipath fading case 3

- **8.9 CPCH Performance**
  - 8.9.3 Demodulation of CPCH message in static propagation conditions
  - 8.9.4 Demodulation of CPCH message in multipath fading case 3

- **8.10 Site Selection Diversity Transmission (SSDT) Mode**
### Signal patterns

For receiver and performance testing for UE

<table>
<thead>
<tr>
<th>Test item Channel combination</th>
<th>Parameter</th>
<th>Palt. name</th>
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<tr>
<td>TS25.101 7 Receiver characteristics</td>
<td>TS25.101 Annex C.3.1</td>
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</tr>
<tr>
<td>TS25.101 Annex A.3.2</td>
<td>D32T18s0</td>
<td>D32T18s8</td>
<td>D32T18s9</td>
</tr>
<tr>
<td>TS25.101 Annex A.3.2</td>
<td>D32T28s0</td>
<td>D32T28s8</td>
<td>D32T28s9</td>
</tr>
<tr>
<td>TS25.101 Annex A.3.3</td>
<td>D32T38s0</td>
<td>D32T38s8</td>
<td>D32T38s9</td>
</tr>
<tr>
<td>TS25.101 Annex A.3.4</td>
<td>D32T48s0</td>
<td>D32T48s8</td>
<td>D32T48s9</td>
</tr>
<tr>
<td>TS25.101 Annex C.4</td>
<td>DL_INTR</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

8.3 Demodulation of DCH in multi-path fading propagation conditions
   - (Case 7) Test 21~25

8.6 Demodulation of DCH in downlink Transmit diversity modes
   - 8.6.1 Demodulation of DCH in open-loop Transmit diversity mode

8.9 Downlink compressed mode

8.10 Blind transport format detection (BTFD)

8.12 Demodulation of Paging Channel (PCH)

7.4 Maximum input level
   - 7.4.2 Maximum input level

9 Performance requirement (HSDPA)
Multi-carrier typical ACLR

- Test Model 1: 64 DPCH, $\leq -8$ dBm
  - -60 dB 5 MHz offset
  - -68 dB 10 MHz offset
Real-time generation of test signal format

- **Simple editing on display**
  - Supporting various test cases
    - Parameters for 5 types of physical channels and 2 types of transport channels

For reference) Mapping relations among main physical channels, transport channels and logical channels
Main physical channels for test

- **P-CPICH** (Primary Common Pilot Channel)
  - Downlink common channel
  - Used as a phase reference for downlink channel estimation

- **S-CPICH** (Secondary Common Pilot Channel)
  - Downlink common channel
  - Used when applying Adaptive Array Antenna
  - Phase reference of S-CPICH during test: P-CPICH180° offset

- **P-CCPCH** (Primary Common Control Physical Channel)
  - Downlink common channel
  - Sends the system and cell information

- **S-CCPCH** (Secondary Common Control Physical Channel)
  - Downlink common channel
  - Sends PCH Paging Channel for paging signal and FACH Forward Access Channel for control information and user data (low rate)

- **PICH** (Page Indication Channel)
  - Downlink common channel
  - Sends Paging indicator for notifying existence of paging to UE

- **P-SCH** (Primary Synchronization Channel)
  - Downlink common channel
  - Used for UE cell search (slot synchronization)

- **S-SCH** (Secondary Synchronization Channel)
  - Downlink common channel
  - Used for UE cell search (frame synchronization and knowing Scrambling code group)
Main physical channels for test

- **DPCH** (Dedicated Physical Channel)
  - Allocated to each UE
  - Downlink: Time multiplexing of DPDCH and DPCCH in time slot
  - Uplink: I/Q multiplexing of DPDCH, DPCCH and HS-DPCCH for HSDPA

- **HS-SCCH** (Shared Control Channel for HS-DSCH)
  - Downlink common channel for HSDPA
  - Maximum of 4 channels per HS-SCCH set
  - Used for HS-PDSCH allocation

- **HS-PDSCH** (High Speed Physical Downlink Shared Channel)
  - Downlink common channel for HSDPA
  - Sends HS-DSCH for packet data
  - Slot format #0: QPSK, 1#: 16QAM

- **OCNS** (Orthogonal Channel Noise Simulator)
  - Interfering channel to simulate other users channels on downlink
Main physical channels for test

- **PRACH** (Physical Random Access Channel)
  - Uplink common channel
  - Sends RACH for control information and user data (low rate)

- **PCPCH** (Physical Common Packet Channel)
  - Uplink common channel
  - Sends CPCH for user packet data (high rate)
Real-time generation of Downlink physical channel

- **P-CCPCH (CH1~3)**
  - BCH transport channel mapping
  - SCH TSDT: On, Off
  - TSDT
    - Time Switched TX Diversity
    - Open loop mode
    - Switching TX antenna (SCH) per slot

- **CPICH (CH1~3)**
  - Antenna: 1,2
    - For TX diversity
    - STTD encoding (Antenna: 2)
    - STTD
      - Space Time Block Coding Based Transmit
      - Antenna Diversity
      - Open loop mode
      - Controlling Symbol patterns on antenna2 side

- **DPCH (CH4)**
  - DCH transport channel mapping
  - Slot format: #0 to #15
  - TPC: TPC command of 4 frames (60 slots) cycle
    - TPC
      - Transmit Power Control
      - Closed loop power control
        - Inner loop power control
        - Controlling to equalize with target SIR
        - Outer loop power control
        - Correcting target SIR to equalize with target BER/BLER
Real-time generation of Uplink physical channel

- DPCCH (CH1~3)
  - Slot format: #0, #2, #5
  - TPC: TPC command of 4 frames (60 slots) cycle
    - TPC
      - Transmit Power Control
      - Closed loop power control
        * Inner loop power control
          Controlling to equalize with target SIR
        * Outer loop power control
          Correcting target SIR to equalize with target BER/BLER

- DPDCH (CH4)
  - DCH transport channel mapping
Real-time generation of Downlink transport channel

- BCH (P-CCPCH data)
  - 3GPP TS 25.944
    - Transport block size: 246
    - CRC: 16 bits
    - Coding: Rate-1/2, Coding rate = 1/2
    - TTI: 20 ms
    - The number of codes: 1
    - SF: 226

- DCH (DPCH data)
  - 3GPP TS 25.101

- BER, BLER
  - Generating the error
  - 0 to 10%, 0.1% resolution
Real-time generation of Uplink transport channel

- **DCH (DPDCH data)**
  - 3GPP TS 25.101

<table>
<thead>
<tr>
<th>Parameters</th>
<th>TrCH1</th>
<th>TrCH2</th>
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<tr>
<td>Transport Block Size</td>
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<td>100</td>
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<tr>
<td>Transport Block Set Size</td>
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<td>100</td>
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<tr>
<td>Transmission Time Interval</td>
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<td>40 ms</td>
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<td>Coding</td>
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<td>Coding Rate</td>
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<td>1/3</td>
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<td>256</td>
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<tr>
<td>Size of CRC</td>
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<td>12</td>
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</tbody>
</table>

- **BER, BLER**
  - Generating the error
  - 0 to 10 %, 0.1 % resolution
Power control function

Operation check of closed loop power control is performable.

- The slot power of each channel is programmable up to 64 slot cycle by editing on display.
  - Editing the slot power for each channel of CH4~12
    - -40 to 0 dB (reference: channel power), 1 dB resolution
- The slot power of each channel is controlled up/down by external control trigger input.
  - Controlling the slot power of specified channel among CH4~12
    - Up & Down in 1, 2 or 3 dB
AWGN mixing

Single unit is performable dynamic range test of BS receiver.

- **Mixing AWGN to Uplink wanted signal**
  - AWGN: Additive White Gaussian Noise
- **High-accuracy and high-stability C/N**
  - -30 to -20 dB, 0.2 dB resolution
  - -19.9 to -8 dB, 0.1 dB resolution

- **Selecting AWGN bandwidth**
  - 1.5×3.84MHz (Chip rate) = 5.76 MHz
  - 2×3.84MHz (Chip rate) = 7.68 MHz
Auxiliary signal Input

» Front panel
  – Data (CH4)
    • Symbol data
  – Clock/Trig
    • Synchronization of external frame clock
    • Frame trigger or start trigger is selectable
      – Used at BS receiver test
  – PWR CONT
    • Refer to “Power Control Function” on previous pages
  – Ref. Clock
    • Synchronization of external baseband reference clock
    • 1×, 2×, 4× chip rate is selectable
      – Used at start trigger
    External reference clock input on rear panel (10/13MHz) is also available
Auxiliary signal

Rear panel
- Data (A),(B), Code I/Q (A),(B)
  - Data & code of CH1~12 are selectable
    - Data: The data before spreading(Symbol) or after spreading(Chip) is selectable
    - At CH1~3
      - (A) Data & code of P-CCPCH and P-SCH
      - (B) Data & code of P-CCPCH and S-SCH
- Reference Clock
  - Baseband reference clock
    - 1x, 2x, 4x, 8x chip rate is selectable
- Symbol Clock, Data Clock

Reference Clock
- Baseband reference clock
  - 1x, 2x, 4x, 8x chip rate is selectable
- Symbol Clock, Data Clock

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MG3681A-E-I-1
MX368141A HSDPA IQproducer™

- MX368141A HSDPA IQproducer™ is the PC application software that generates 3GPP HSDPA compliant signal patterns outputted from MG3681A Digital Modulation Signal Generator.
- MG3681A Digital Modulation Signal Generator that has MU368040A CDMA MODULATION UNIT and MX368041B W-CDMA Software is required for the use of generated signal patterns.
- Since multiple pattern files that are generated can be downloaded into MG3681A mainframe, users can switch over signal patterns easily by selecting them.
Easy to generate signal patterns with the setting file included

- With the MX368141A HSDPA IQproducer™, users can generate signal patterns by editing a setting file (csv format) that determines HSDPA-system signal patterns with Excel program and converting the edited setting file.
- With the setting file of standard signal patterns (Fixed Reference Channel*) included in the software, users can generate signal patterns easily only by editing the parameter they wish to change.

MX368141A HSDPA IQproducer™
setting file edit screen

MX368141A HSDPA IQproducer™
setting file convert screen
Operating environment

Personal computer
- **OS:** Windows 2000/XP
- **CPU:** Pentium 300MHz or faster
- **Memory size:** ≥128MB
- **HDD:** Occupation ≤200MB
- **Display:** 800×600 pixels or more
- **Peripheral equipment:**
  - It be possible to read CD-R.
  - It be possible to save in Compact-Flash (PC card adapter is required for download to MG3681A)
Comparison of MX368141A HSDPA IQproducer and MX368041A-11 HSDPA signal pattern

The functional difference about HSDPA

<table>
<thead>
<tr>
<th>Model</th>
<th>MG3681A</th>
<th>MG3681A</th>
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<tr>
<td>- Baseband</td>
<td>- MU368040A</td>
<td>- MU368040A</td>
</tr>
<tr>
<td>- Software</td>
<td>- MX368041A/B</td>
<td>- MX368041A/B</td>
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<tr>
<td>- HSDPA application software</td>
<td>- MX368141A</td>
<td>- MX368041A/B-11</td>
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<table>
<thead>
<tr>
<th>Type of software</th>
<th>IQproducer</th>
<th>Signal pattern</th>
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<tbody>
<tr>
<td>* Change of a parameter is</td>
<td>* Change of a parameter is</td>
<td>possible.</td>
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</table>

<table>
<thead>
<tr>
<th>Component test for Down-Link of HSDPA</th>
<th>No</th>
<th>Yes</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Supports test model 5)</td>
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<table>
<thead>
<tr>
<th>Component test for Up-Link of HSDPA</th>
<th>Yes</th>
<th>No</th>
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<tbody>
<tr>
<td>(Supports HS-DPCCH)</td>
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<table>
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<th>Supports HSDPA channels</th>
<th>HS-PDSCH</th>
<th>HS-PDSCH</th>
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</thead>
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<tr>
<td>HS-SCCH</td>
<td>HS-SCCH</td>
<td></td>
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<tr>
<td>HS-DPCCH</td>
<td></td>
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</tbody>
</table>

MX368141A can change a parameter and supports HS-DPCCH of HSDPA Uplink.
MX368040A-11 support "Test Model 5" of the component test of HSDPA Downlink.
MX368042A IS-95 Device Test Software

- Forward/Reverse cdmaOne test signals for IS-95A/B (3GPP2 C.S0002 RC1 & 2) standard can be outputted by installing the MX368042A IS-95 Device Test Software in the MU368040A CDMA Modulation Unit.
- In R&D/production process of components, base stations (BS) and mobile stations (MS), the functions to support various applications are provided as the signal source for components and the interfering signal source for receiver test.
Generation of test signal format

- Test Mode 1 & 2 signals in IS-97A/B (3GPP2 C.S0010 RC1 & 2) test specifications can be simply set without setting complicated parameters of IS-95A/B (3GPP2 C.S0002 RC1 & 2).

Caution

» Channel coding is not supported (FER Frame Error Rate test is not performable)

- DSP stores the I/Q mapping data of 98304 chip (4 frames) /4× over sampling in Waveform data Memory according to the parameter set on display.

<table>
<thead>
<tr>
<th>Channel Type</th>
<th>Number of Channels</th>
<th>Fraction of Power (I/Q)</th>
<th>Fraction of Power (dB)</th>
<th>Comments</th>
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<tbody>
<tr>
<td>Forward Pilot</td>
<td>1</td>
<td>0.2000</td>
<td>-7.0</td>
<td>Code channel W_{0}^{138}</td>
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<td>Sync</td>
<td>1</td>
<td>0.0471</td>
<td>-13.3</td>
<td>Code channel W_{32}^{54}; always L/8 rate</td>
</tr>
<tr>
<td>Paging</td>
<td>1</td>
<td>0.1882</td>
<td>-7.3</td>
<td>Code channel W_{1}^{96}; full rate only</td>
</tr>
<tr>
<td>Traffic</td>
<td>6</td>
<td>0.09412</td>
<td>-10.3</td>
<td>Variable code channel assignments; full rate only</td>
</tr>
</tbody>
</table>

DSP functional block diagram
Generation of test signal format

- Simple editing on display
  - Support various test cases

<table>
<thead>
<tr>
<th>Channel Type</th>
<th>Walsh Code</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pilot</td>
<td>0</td>
<td>Symbol Data is &quot;0&quot;.</td>
</tr>
<tr>
<td>Sync</td>
<td>32</td>
<td>Symbol Data is Random.</td>
</tr>
<tr>
<td>Paging</td>
<td>1 to 7</td>
<td>Symbol Rate is 3.8 kbps.</td>
</tr>
<tr>
<td>Traffic</td>
<td>8 to 31, 33 to 63</td>
<td>Symbol Data is Random.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Symbol Rate is 99.2 kbps.</td>
</tr>
</tbody>
</table>

Forward
- Multiple channels
  - 1 to 64
- Per Walsh code (0 to 63)
  - On, Off, OCNS
  - Code Domain Power
    - -40 to 0 dB, 0.1 dB resolution
- Traffic channels
  - Rate set
    - 1 (RC1), 2 (RC2)
  - Data rate
    - Full, Half, Quarter, Eighth
      - 9.6, 4.8, 2.4, 1.2 kbps (Rate set 1)
      - 14.4, 7.2, 3.6, 1.8 kbps (Rate set 2)

Reverse
- Data rate
  - Full, Half, Quarter, Eighth
    - 9.6, 4.8, 2.4, 1.2 kbps (Rate set 1)

Discover What’s Possible™
Peak Clipping of test signal

- Useful for the evaluation of crest factor (CCDF) at components
  - Limiting the peak level of I/Q amplitude
Peak Clipping of test signal

- **Clipping before FIR filtering**
  - ACLR of output signals is not deteriorated because of no distortion caused by clipping.
  - Extreme clipping deteriorates waveform quality.
  - FIR filtering may cause the peak exceeding limited level. Large peak is caused especially at few multiplex number.

- **Clipping after FIR filtering**
  - Clipping causes distortion and deteriorates the ACLR of output signals.

- **Scalar clipping**
  - Limiting I or Q amplitude level

- **Vector clipping**
  - Limiting RMS $\sqrt{(I^2+Q^2)}$ level
Peak Clipping Monitor of test signal

- “Clipping” is indicated when vector amplitude is attenuated by Clipping
  » Selectable “Clipping Monitor”

- Checking Attenuated time and vector amplitude
  » Clipped Time Rate
    - Percentage of attenuated sampling point
  » Clipped Max Ratio
    - Attenuation percentage of max. vector amplitude

- 100% indicates the vector amplitude without attenuation
Auxiliary signal Output

» Rear panel
  – Reference Clock
    • Baseband reference clock
    – Chip rate
  – Timing Clock
    • 20ms, 26.7ms, 80ms, 2sec is selectable
MX368011A PDC Software

- Downlink/Uplink PDC test signals (TCH, VOX) for RCR STD-27 standard can be outputted by installing the MX368011A PDC Software in the MU368010A TDMA Modulation Unit.
- In R&D/production process of components, base stations (BS) and mobile stations (MS), the functions to support various applications are provided as the signal source for components, the wanted signal source and the interfering signal source for receiver test.
Emulation of MG3670 series

MG3670 series/MG3660A
- MG0301C $\pi/4$DQPSK Modulation Unit
- MG0303B Burst Function Unit

Equal functions
- Display
- Remote control
Real-time generation of test signal format

- **Simple editing on display**
  - Support various test cases
  - Full rate/Half rate
  - Slot On/Off
  - Parameter

- **PRBS data of TCH**
  - Continuous in the same slot
  - Phase is shifted per slot
    - When invalid slot is received, PRBS data becomes discontinuous and detectable by BER test
Real-time generation of test signal format

- **VOX** (Voice Operated Transmission)
  - Controlling to transmit voice signal in voice period and not to transmit voice signal in voiceless period for power saving of MS.

- Interfering signal for receiver test
Pattern memory (MU368010A internal memory)

- Parameter settings up to 100 types on Pattern Edit screen can be saved.
- Title up to 8 characters can be inputted for easy confirmation.

» Saved parameter setting window
External data input

π/4DQPSK modulation signal of arbitrary frame format can be outputted by utilizing the pulse pattern generator.
Auxiliary signal Input

» Front panel
  – Data, Symbol Clock, Burst Gate, Data Clock
    • Refer to “External Data Input” on previous pages
  – Burst Trig
    • Synchronization of external burst trigger
      – Used at BS receiver test
**Auxiliary signal**

- **Rear panel**
  - Data, Data Clock, Symbol Clock
  - Pattern Sync
    - PN Clock, PN Gate, RF Gate is selectable
  - at Burst On
  - Burst Gate

- **Output**
  - Burst Trigger
    - Full/Half rate: 20 / 40 ms clock

---

**Control signal of internal pulse modulator**
MX368012A GSM Device Test Software

- Downlink/Uplink GSM test signals (NB Normal Burst, AB Access Burst) for 3GPP TS (GSM) 05.01 standard can be outputted by installing the MX368012A GSM Device Test Software in the MU368010A TDMA Modulation Unit.

- In R&D/production process of components, base stations (BS) and mobile stations (MS), the functions to support various applications are provided as the signal source for components and the interfering signal source for receiver test.
Emulation of MG3670 series

MG3670 series/MG3660A
- MG0302A GMSK Modulation Unit
- MG0303B Burst Function Unit

Equal functions
- Display
- Remote control

Additional function
- RACH format
  » Access Burst
Real-time generation of test signal format

- **Simple editing on display**
  - Support various test cases
  - Slot On/Off
  - Slot level
    - -20 to 0 dB, 0.1 dB resolution
  - Differential Encode
    - Differential encoding in 3GPP TS (GSM) 05.04
  - Parameter

- **PRBS data of $E$ (Encrypted bits)**
  - Continuous in the same slot
  - Phase is shifted per slot
    - When invalid slot is received, PRBS data becomes discontinuous and detectable by BER test

![Diagram]

---

Discover What’s Possible™

Slide 94
MG3681A-E-I-1
Real-time generation of test signal format

- Interfering signal for receiver test
Channel coding of test signal format

Caution

» 3GPP TS (GSM) 05.03 Channel Coding is not supported.
  - Traffic Channels (TCH)
    • TCH/FS (Speech channel at full rate)
    • TCH/EFS (Speech channel at enhanced full rate)
  - Control Channels
    • SACCH (Slow associated control channel)
    • RACH (Random access channel)
  - Packet Switched Channels
    • PDTCH (Packet data traffic channel)

» Multiframe format is not supported.

(a) \[\text{T T T T T T T T T T T A T T T T T T T T T T T T T T T T T T T T} \]

\[\text{26 frames } = 120 \text{ ms}\]

(b) \[\text{T t T t T t T t T t T t A T t T t T t T t T t T t T t T t a} \]

(a) case of one full rate TCH
T, t: TDMA frame for TCH
-: idle TDMA frame

(b) case of two half rate TCHs
A, a: TDMA frame for SACCH/T
Time slot configuration in 3GPP TS 05.01

1 hyperframe = 2 048 superframes = 2,715,648 TDMA frames (3 hours 28 minutes 53 seconds 760 milliseconds)

1 superframe = 1,326 TDMA frames (6.12 seconds)

1 (26-frame) multiframe = 26 TDMA frames (120 milliseconds)

1 (51-frame) multiframe = 51 TDMA frames (3060/13 milliseconds)

1 TDMA frame = 8 time slots (120/26 or 4.615 milliseconds)

1 time slot = 156.25 symbol durations (15/26 or 0.577 milliseconds)

(1 symbol duration = 48/13 or 3.69 microseconds)

NOTE: GMSK modulation: one symbol is one bit
8PSK modulation: one symbol is three bits

Normal burst (NB) The number shown are in symbols

Frequency correction burst (FB)

Synchronization burst (SB)

Access burst (AB)

Discover What’s Possible™

Slide 97
MG3681A-E-I-1
Pattern memory (MU368010A internal memory)

- Parameter settings up to 100 types on Pattern Edit screen can be saved.
- Title up to 8 characters can be inputted for easy confirmation.

» Saved parameter setting window
External data input

GMSK modulation signal of arbitrary frame format can be outputted by utilizing the pulse pattern generator.
Auxiliary signal Input

» Front panel
  - Data, Burst Gate, Data Clock
    • Refer to “External Data Input” on previous pages
  - Symbol Clock
    • Same as Data Clock
  - Burst Trig
    • Synchronization of external burst trigger
      - Used at BS receiver test
Auxiliary signal

Rear panel
- Data, Data Clock
  - Symbol Clock is the same as Data Clock
- Pattern Sync
  - PN Clock, PN Gate, RF Gate is selectable at Burst On
- Burst Gate
- Burst Trigger
  - 4.615 ms clock

Output

Control signal of internal pulse modulator

Data, Symbol Clock, Burst Gate, Burst Trigger, Data Clock, I/O Input

Digital Output
A1: Data Clock
A2: Symbol Clock
B1: Burst Gate
B2: Pattern Sync
B3: PN Clock, PN Gate, RF Gate

Digital Input/Output
C1
C2
C3
C4
D1
D2
D3

Data: 0-2S
4S: 10-14
24 & 2S: Ground
MX368031A Device Test Signal Generation Software

- The test signals for worldwide main communications systems can be outputted by installing the MX368031A Device Test Signal Generation Software in the MU368030A Universal Modulation Unit.
- In production process of components, the function is provided as the signal source for components.
- In production process of CDMA2000 1X BS, the function is provided as the wanted signal source for receiver test.
- In R&D/production process of CDMA2000 1X MS, CDMA2000 1xEV-DO AN Access Network and AT Access Terminal, the function is provided as the interfering signal source for receiver test.
Support of test signal format

- Just to select the signal patterns saved in large-capacity waveform memory without setting complicated parameters of communication systems! **Simple operation**
- **High-speed change** among TDMA 5 signal patterns and CDMA2000 10 signal patterns < 1 sec
  - TDMA: GSM/EDGE (2), PDC, IS-136, PHS
  - CDMA2000: CDMA2000 1X (5), 1xEV-DO (4)
- **Quick support** is provided by updating the signal pattern files saved from PC memory card to internal memory.
  - IQ signal pattern file is downloaded to MG3681A via PC memory card (CompactFlash).
    - The I/Q mapping data of over sampling is stored in Waveform data Memory.
Signal patterns

- **TDMA**
  - Frame coding -not supported
  - GSM/EDGE: 8PSK PN9 cont. modulation, Linearized Gaussian, 270.833ksps
  - GSM/EDGE: GMSK PN9 cont. modulation, Gaussian (Bbt: 0.3), 270.833ksps
  - PDC: π/4DQPSK PN9 cont. modulation, Root Nyquist (α: 0.5), 21ksps
  - NADC(IS-136): π/4DQPSK PN9 cont. modulation, Root Nyquist (α: 0.35), 24.3ksps
  - PHS: π/4DQPSK PN9 cont. modulation, Root Nyquist (α: 0.5), 192ksps

- **CDMA2000 1X**
  - Reverse: Channel coding -supported (Utilizable for FER test of BS)
    - RC1: BPSK→OQPSK Traffic(TCH)
    - RC3 (1): BPSK→HPSK Fundamental(FCH) + Pilot(PICH)
    - RC3 (2): BPSK→HPSK Fundamental(FCH) + Supplemental(SCH) + Pilot(PICH)
    - RC3 (3): BPSK→HPSK Dedicated Control(DCCH) + Pilot(PICH)
  - Forward: Channel coding -not supported
    - RC1-2: BPSK→QPSK Pilot(PICH) + SYNC + Paging(PCH) + Traffic(TCH)x6
    - RC3-5: BPSK/QPSK→QPSK Pilot(PICH) + SYNC + Paging(PCH) + Traffic(TCH)x6

- **CDMA2000 1xEV-DO**
  - Channel coding -not supported
    - Forward:
      - Active Slot: BPSK/16QAM→QPSK Pilot(PICH) + MAC + Data
      - Idle Slot: BPSK→QPSK Pilot(PICH) + MAC
    - Reverse:
      - 9.6 kbps: BPSK→HPSK Pilot(PICH) + DRC + ACK + Data
      - 153.6 kbps: BPSK→HPSK Pilot(PICH) + DRC + ACK + Data
      - 153.6 kbps: BPSK→HPSK Pilot(PICH) + DRC + ACK + Data

PDC, GSM, PHS

**Identical signal patterns**

**MX368031A**

- **PDC**
  - Baseband: 10/11/20
  - I/O Mod.: [Int]
  - Pulse Mod.: [Int]
  - System: [PDC]
  - Pattern: [MX368011A (PDC)]
  - Baseband Setup:
    - Trigger Source: [Int]
    - Trigger Delay: 0.016666666666666666
    - Reference Clock: [Int]

**MX368031A**

- **GSM**
  - Baseband: 10/11/20
  - I/O Mod.: [Int]
  - Pulse Mod.: [Int]
  - System: [GSM]
  - Pattern: [MX368012A (GSM)]
  - Baseband Setup:
    - Trigger Source: [Int]
    - Trigger Delay: 0.000000
    - Reference Clock: [Int]

**MX368031A**

- **PHS**
  - Baseband: 10/11/20
  - I/O Mod.: [Int]
  - Pulse Mod.: [Int]
  - System: [PHS]
  - Pattern: [MX368035A (PHS)]
  - Baseband Setup:
    - Trigger Source: Int
    - Reference Clock: [Int]
CDMA2000 1X Identical signal patterns

MX368031A

» CDMA2000 1X
  – Forward RC1-2

MX368042A (IS-95)
CDMA2000 1xEV-DO
MX368031A

» CDMA2000 1xEV-DO
- Forward Active Slot

Baseband : [On ]
I/O Mod. : [Int] Pulse Mod. : [Int]
System : [CDSS]
Pattern : [EV-DO.PAD]
Baseband Setup
Trigger Source : [Int ] Trigger Delay : [ 0] 0.0000  kbps
Reference Clock : [Int ]

- Forward Idle Slot

Baseband : [On ]
I/O Mod. : [Int] Pulse Mod. : [Int]
System : [CDSS]
Pattern : [EV-DO.PAD.100]
Baseband Setup
Trigger Source : [Int ] Trigger Delay : [ 0] 0.0000  kbps
Reference Clock : [Int ]

- Reverse 9.6 kbps

Baseband : [On ]
I/O Mod. : [Int] Pulse Mod. : [Int]
System : [CDSS]
Pattern : [EV-DO.RVS.9.6]
Baseband Setup
Trigger Source : [Int ] Trigger Delay : [ 0] 0.0000  kbps
Reference Clock : [Int ]

- Reverse 153.6 kbps

Baseband : [On ]
I/O Mod. : [Int] Pulse Mod. : [Int]
System : [CDSS]
Pattern : [EV-DO.RVS]
Baseband Setup
Trigger Source : [Int ] Trigger Delay : [ 0] 0.0000  kbps
Reference Clock : [Int ]

Identical signal patterns

» MX368033A (1xEV-DO)

Baseband : [On ]
I/O Mod. : [Int] Pulse Mod. : [Int]
System : [1xEV-DO]
Pattern : [1xEV-DO.1.128]
Baseband Setup
Trigger Source : [Int ] Trigger Delay : [ 0] 0.0000  kbps
Reference Clock : [Int ]

- Forward Idle Slot

Baseband : [On ]
I/O Mod. : [Int] Pulse Mod. : [Int]
System : [1xEV-DO]
Pattern : [1xEV-DO.1.128.100]
Baseband Setup
Trigger Source : [Int ] Trigger Delay : [ 0] 0.0000  kbps
Reference Clock : [Int ]

- Reverse 9.6 kbps

Baseband : [On ]
I/O Mod. : [Int] Pulse Mod. : [Int]
System : [1xEV-DO]
Pattern : [1xEV-DO.9.6]
Baseband Setup
Trigger Source : [Int ] Trigger Delay : [ 0] 0.0000  kbps
Reference Clock : [Int ]

- Reverse 153.6 kbps

Baseband : [On ]
I/O Mod. : [Int] Pulse Mod. : [Int]
System : [1xEV-DO]
Pattern : [1xEV-DO.153.6]
Baseband Setup
Trigger Source : [Int ] Trigger Delay : [ 0] 0.0000  kbps
Reference Clock : [Int ]
Auxiliary signal Input

» Front panel
  – Trigger
    • Available at CDMA2000 1X Reverse signal
    • Synchronization of external frame clock
    • Frame trigger or start trigger is selectable
      – Used at BS receiver test
  – Ref. Clock
    • Available at CDMA2000 signal
    • Synchronization of external baseband reference clock
    • \(8 \times\) chip rate \((8 \times 1228.4 \text{ kcps} = 9830.4 \text{ kHz})\)
      – Used at start trigger
    External reference clock input on rear panel \((10/13\text{MHz})\) is also available
Auxiliary signal

- Rear panel
  - RF Gate
    - 1xEV-DO Idle slot (Burst)
  - Sampling Clock
    - Available at CDMA2000 signal
    - Baseband reference clock
      - $8 \times$ chip rate
        $8 \times 1228.4$ kcps $= 9830.4$ kHz

Control signal of internal pulse modulator

Output

- Digital Output
  - A1: RF Gate
  - A2: Frame Trigger
  - B1: Sampling Clock
  - B2: Sequence Pulse
  - B4:
- Digital Input/Output
  - C1:
  - C2:
  - C3:
  - C4:
  - D1:
  - D2:
- AUX 1
  - AUX 2

Diagram of rear panel with connections and labels.
» Rear panel
  – Frame Trigger, Sequence Pulse
    – CDMA2000 1X

Auxiliary signal

Output

– 1xEV-DO (Active/Idle)

– 1xEV-DO Reverse
MX368033A CDMA2000 1xEV-DO Signal Generation Software

- Forward/Reverse CDMA2000 1xEV-DO test signals for 3GPP2 C.S0024 standard can be outputted by installing the MX368033A CDMA2000 1xEV-DO Signal Generation Software in the MU368030A Universal Modulation Unit.
- In R&D/production process of components, AN Access Network and AT Access Terminal, the functions to support various applications are provided as the signal source for components and the wanted signal source for receiver test.
Support of test signal format

- Receiver test (PER Packet Error Rate) for 3GPP2 C.S0032 (Sector) and C.S0033 (AT) test specifications is performable due to the Coding format (Frame/Slot structuring, CRC addition, turbo coding, interleave) based on 3GPP2 C.S0024.
- Just to select the signal patterns saved in large-capacity waveform memory without setting complicated parameters of 3GPP2! Simple operation
- High-speed change among Forward 13 data rate signal patterns (with Idle Slot) and Reverse 5 data rate signal patterns < 1 sec
- Supporting multi-carrier up to 8×
- Quick support is provided by updating the signal pattern files saved from PC memory card to internal memory.
  - IQ signal pattern file is downloaded to MG3881A via PC memory card (CompactFlash).
    - The I/Q mapping data of 8× over sampling is stored in Waveform data Memory.
    - 16× over sampling at multi-carrier
**Signal patterns**

- **Forward (13 patterns)**
  - for receiver test of Sector
  - for transmitter test of AT

- **Reverse (10 patterns)**
  - for receiver test of Sector
  - for transmitter test of AT

### Signal Patterns Table

<table>
<thead>
<tr>
<th>Data Rate (kbps)</th>
<th>9.6</th>
<th>19.2</th>
<th>38.4</th>
<th>76.8</th>
<th>153.6</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reversed Rate Index</td>
<td>1</td>
<td>2</td>
<td>3</td>
<td>4</td>
<td>5</td>
</tr>
<tr>
<td>Code Rate</td>
<td>1/4</td>
<td>1/4</td>
<td>1/4</td>
<td>1/4</td>
<td>1/2</td>
</tr>
<tr>
<td>Bits per Physical Layer Packet</td>
<td>256</td>
<td>512</td>
<td>1,024</td>
<td>2,048</td>
<td>4,096</td>
</tr>
<tr>
<td>Number of Turbo Encoder Input Symbols</td>
<td>250</td>
<td>506</td>
<td>1,018</td>
<td>2,042</td>
<td>4,090</td>
</tr>
<tr>
<td>Turbo Encoder Code Rate</td>
<td>1/4</td>
<td>1/4</td>
<td>1/4</td>
<td>1/4</td>
<td>1/2</td>
</tr>
<tr>
<td>Encoder Output Block Length (Code Symbols)</td>
<td>1,024</td>
<td>2,048</td>
<td>4,096</td>
<td>8,192</td>
<td>8,192</td>
</tr>
</tbody>
</table>

---

**Data Rate (kbps)**

<table>
<thead>
<tr>
<th>Data Rate (kbps)</th>
<th>38.4</th>
<th>76.8</th>
<th>153.6</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Values per Physical Layer Packet</td>
<td>1,024</td>
<td>3,072</td>
<td>4,096</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Data Rate (kbps)</th>
<th>307.2</th>
<th>614.4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Values per Physical Layer Packet</td>
<td>128</td>
<td>64</td>
</tr>
</tbody>
</table>
Multi-carrier

Multi-carrier are stored in PC memory card as sample signal patterns.

– Forward Active Slot multi-carrier (8×, 4×, 3×, 2×, 1×)
– Forward Idle Slot multi-carrier (8×, 4×, 3×, 2×, 1×)
  • Frequency offset: 1.25 MHz
  • Pilot Channel:
    – PN Offset Index = 0 (f1), 1 (f2), 2 (f3), 3 (f4), 4 (f5), 5 (f6), 6 (f7), 7 (f8)
  • MAC Channel:
    – MACIndex = RA, 13 RPC

\[
\begin{array}{cccccccccc}
\text{f1} & \text{f2} & \text{f3} & \text{f4} & \text{f5} & \text{f6} & \text{f7} & \text{f8} \\
\end{array}
\]

– RABit = PRBS
– RPCBit = PRBS

• Frame length: 3 frame (Active Slot), 1 frame (Idle Slot)

Active Slot
• Traffic Channel: PN15fix
• Data Rate: 2457.6 kbps
• Preamble: 64 chip
• Modulation: 16QAM
Multi-carrier select

Downloading the signal pattern file from PC memory card

Forward Active slot

Reverse (appendix)

Forward Idle slot
4 carriers Spurious Emissions (typ.)

### Forward Active Slot

<table>
<thead>
<tr>
<th></th>
<th>L* / U* dBc/30kHz</th>
<th></th>
<th>L* / U* dBc/30kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>1:</td>
<td>-69.35 / -70.81</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2:</td>
<td>-73.78 / -74.87</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3:</td>
<td>-74.96 / -75.36</td>
</tr>
</tbody>
</table>

### Forward Idle Slot

<table>
<thead>
<tr>
<th></th>
<th>L* / U* dBc/30kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>1:</td>
<td>-64.76 / -62.59</td>
</tr>
<tr>
<td>2:</td>
<td>-70.35 / -70.83</td>
</tr>
<tr>
<td>3:</td>
<td>-70.54 / -72.24</td>
</tr>
</tbody>
</table>

L3 L2 L1 U1 U2 U3
AWGN mixing

Single unit is performable dynamic range test of BS receiver.
• Mixing AWGN to CDMA2000 wanted signal
• High-accuracy and high-stability C/N
  » -30 ~ -30 dB, 0.1 dB resolution

• Selecting AWGN bandwidth
  » 2× 1.23MHz = 2.46 MHz
  » 3× 1.23MHz = 3.69 MHz
  » 4× 1.23MHz = 4.92 MHz
Auxiliary signal Input

» Front panel
  – Trigger
    • Synchronization of external frame clock
    • Frame trigger or start trigger is selectable
      – Used at Sector receiver test
  – Ref. Clock
    • Available at single carrier
    • Synchronization of external baseband reference clock
    • $8 \times$ chip rate ($8 \times 1228.4$ kcps = $9830.4$ kHz)
      – Used at start trigger
    External reference clock input on rear panel (10/13MHz) is also available
Rear panel
  - RF Gate
    - Forward Idle slot (Burst)
  - 8x Chip Clock
    - Available at single carrier
    - Baseband reference clock
      - 8x chip rate
        (8x 1228.4 kcps = 9830.4 kHz)
  - Frame Trigger, Sequence Pulse
    - Forward (Active/Idle)
  - Reverse

Control signal of internal pulse modulator

Digital Output
  - A1: RF Gate (M.P. 4)
  - B1: 8x Chip Clock
  - B2: Sequence Pulse

Digital Input/Output
  - C1: Frame Trigger
  - C2: B1
  - D1: B2
  - D2: C3

Switch 25
  - X1: 1
  - X2: 2
  - X3: 3
  - X4: 4
  - X5: 5
  - X6: 6
  - X7: 7
  - X8: 8
  - X9: 9
  - X10: 10
  - X11: 11
  - X12: 12
  - X13: 13
  - X14: 14
  - X15: 15
  - X16: 16
  - X17: 17
  - X18: 18

Frame Trigger

Sequence Pulse

RF Output

Output timing at start of PN150

Discover What’s Possible™

MG3681A-E-I-1

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MX368133A CDMA2000 1xEV-DO IQproducer™

- It is Windows application software which upgrades the functioning of MX368033A installed in the MG3681A.
- The IQ mapping data file for signal patterns, which are generated by MU368030A Universal Modulation Unit incorporated in the MG3681A is created.
- In R&D process of components, AN and AT, the functions to perform various evaluation of power amplifier and demodulation test are supported.
Reference setting files for easy setup

- Since the reference setting files for signal patterns of standard MX368033A is recorded, a signal pattern can be created easily only by editing a parameter changing.

 Forward Traffic Channel frame (26.66... ms)

- PN Offset Index
- Data
- MAC
- MAC
- MAC
- MAC
Editing of various MAC channels

- Able to edit parameters for each frame and slot
- Multiplex of RA channels and RPC channels

### Random bits

<table>
<thead>
<tr>
<th>MAC Index</th>
<th>MAC Channel Use</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 and 1</td>
<td>Not Used</td>
</tr>
<tr>
<td>2</td>
<td>Not Used</td>
</tr>
<tr>
<td>3</td>
<td>Not Used</td>
</tr>
<tr>
<td>4</td>
<td>RA Channel</td>
</tr>
<tr>
<td>5-63</td>
<td>Available for RPC Channel and DRChannel Transmissions</td>
</tr>
</tbody>
</table>
Creating Forward multi-carrier

- Able to edit parameters for each carrier
  - 1 ~ 9

- Up to 9 carriers
  - 1.25MHz offset

- Calculating the IQ mapping data
- Creating 3 files
  - I data
  - Q data
  - Configuration file for download
Signal pattern combiner

- Performable high-speed change of signal pattern

Created signal pattern files

- ***I.dlw
- ***Q.dlw
- UMU33***.dli

Combined signal pattern file

- ???I.dlw
- ???Q.dlw
- UMU33???.dli (Rename)
Operating requirements

Personal computer
- **OS:** Windows 2000, XP **recommendation**
- **CPU:** $\geq 300\text{MHz}$
- **Memory:** $\geq 128\text{MB} \hspace{1cm} \text{recommendation}$
- **HDD:** $\leq 512\text{MB} \hspace{1cm} \text{Occupied}$
- **Display:** $\geq 800\times600\text{ pixel}$
- **Peripheral equipment:**
  - Reading CD-R
  - Saving to PC memory card(CompactFlash+PC card adapter)
  - Storing I/Q mapping data to Waveform data Memory of MU368030A
MX368034A PDC Packet Software

- Downlink/Uplink PDC user packet channel (UPCH) test signals for RCR STD-27 standard can be outputted by installing the MX368034A PDC Packet Software in the MU368030A Universal Modulation Unit.
- In R&D/production process of components, base stations (BS) and mobile stations (MS), the functions to support various applications are provided as the signal source for components and the wanted signal source for receiver test.
Support of test signal format

- Packet (Downlink up to 28.8 kbps) receiver test (BER) for BS/MS is performable due to the Frame/Slot format based on RCR STD-27.
- Just to select the signal patterns saved in large-capacity waveform memory without setting complicated parameters of RCR STD-27! Simple operation
- Changing among Downlink 3 data rate signal patterns and Uplink 1 data rate signal pattern (approx. 10 min)
- UPCH ⇔ TCH (MX368011A) High-speed change < 10 sec
- Quick support is provided by updating the waveform data saved from PC memory card to internal memory.
  - IQ signal pattern file is downloaded to MG3681A via PC memory card (CompactFlash).
    - The I/Q mapping data of 16× over sampling is stored in Waveform data Memory.
Signal patterns frame configuration

- Physical channel for packet communication (UPCH)

Patterns

- Downlink 3 slots
- Downlink 2 slots
- Downlink 1 slot
- Uplink 1 slot

- Super-frame is not supported
**Signal patterns slot configuration**

- **Downlink physical channel for packet communication (UPCH)**
  - 280 bit
    - Scrambling Off

<table>
<thead>
<tr>
<th>R</th>
<th>P</th>
<th>CAC</th>
<th>SW</th>
<th>CC</th>
<th>CAC</th>
<th>E</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>2</td>
<td>112</td>
<td>20</td>
<td>8</td>
<td>112</td>
<td>22</td>
</tr>
</tbody>
</table>

- R  Guard time for burst transient response 0000
- P  Preamble 10
- SW Synchronous word
  - Slot 0: S1(87A4B)
  - Slot 1: S2(9D236)
  - Slot 2: S3(81D75)
- CC Color code 00000000
- E Collision control bit
**Signal patterns**

**slot configuration**

- **Uplink physical channel for packet communication (UPCH)**
  - 280 bit
    - Scrambling Off

<table>
<thead>
<tr>
<th>R</th>
<th>P</th>
<th>CAC</th>
<th>SW</th>
<th>CC</th>
<th>CAC</th>
<th>G</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>2</td>
<td>112</td>
<td>20</td>
<td>8</td>
<td>116</td>
<td>18</td>
</tr>
</tbody>
</table>

- R  Guard time for burst transient response 0000
- P  Preamble 10
- SW Synchronous word
  - Slot 0: S1'(785B4)
- CC Color code 00000000
- G  Guard time
Auxiliary signal Input

» Front panel
   – Trigger
     • Synchronization of external frame clock
     • Frame trigger or start trigger is selectable
       – Used at BS receiver test
   – Ref. Clock
     • Synchronization of external baseband reference clock
     • 16× symbol rate (16× 21 ksp = 336 kHz)
       – Used at start trigger
       External reference clock input on rear panel (10/13MHz) is also available
Rear panel
- RF Gate
  - Uplink (Burst)
- 16x Symbol Clock
  - Baseband reference clock
    - 16x symbol rate
      (16× 21 kps = 336 kHz)
- Frame Trigger, Sequence Pulse
  - Downlink
  - 2044 frames
  - 10220 ms
- Uplink
  - 511 frames
  - 10220 ms
MX368035A PHS Signal Generation Software

- Downlink/Uplink PHS test signals (TCH) for RCR STD-28 standard can be outputted by installing the MX368035A PHS Signal Generation Software in the MU368030A Universal Modulation Unit.
- In R&D/production process of components, CS and PS, the functions to support various applications are provided as the signal source for components, the wanted signal source and the interfering signal source for receiver test.

![Signal Generation Software Interface](image-url)
Support of test signal format

- Receiver test (BER) for CS/PS test specifications is performable due to the $\pi/4$DQPSK Frame/Slot format based on RCR STD-28 Version 4.0.
- Just to select the signal patterns saved in large-capacity waveform memory without setting complicated parameters of RCR STD-28!

Simple operation

- **High-speed change** the signal patterns < 1 sec
- Continuous modulated signal patterns for Advanced PHS on RCR STD-28 Version 4.0 are appended as sample file.

<table>
<thead>
<tr>
<th></th>
<th>16QAM</th>
<th>8PSK</th>
<th>QPSK</th>
<th>BPSK</th>
<th>kHzBW</th>
<th>ksp</th>
<th>$\alpha$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1x:</td>
<td>PN9/15</td>
<td>PN9/15</td>
<td>PN9/15</td>
<td>PN9/15</td>
<td>288</td>
<td>192</td>
<td>0.5</td>
</tr>
<tr>
<td>3x:</td>
<td>PN9/15</td>
<td>PN9/15</td>
<td>PN9/15</td>
<td>PN9/15</td>
<td>884</td>
<td>640</td>
<td>0.38</td>
</tr>
</tbody>
</table>

- **Quick support** is provided by updating the signal pattern files saved from PC memory card to internal memory.
  - IQ signal pattern file is downloaded to MG3681A via PC memory card (CompactFlash).
    - The I/Q mapping data of 20× over sampling is stored in Waveform data Memory.
Signal patterns frame configuration

- $\pi/4$DQPSK Traffic channel (TCH)
  - Downlink/Uplink 1 slot

  Slot 1 | Slot 2 | Slot 3 | Slot 4

  ▶ 5 ms

- $\pi/4$DQPSK PN9 continuous modulation
  - for the wanted signal source for receiver test

- $\pi/4$DQPSK PN9 continuous modulation
  - for the signal source for components

- $\pi/4$DQPSK PN15 continuous modulation
  - for the interfering signal source for receiver test

- Super-frame is not supported

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Anritsu
Signal patterns slot configuration

- \(\pi/4\)DQPSK Traffic channel (TCH)
  - 240 bit, 625 ms
    - Scrambling Off

<table>
<thead>
<tr>
<th>R</th>
<th>SS</th>
<th>PR</th>
<th>UW</th>
<th>CI</th>
<th>SA</th>
<th>TCH</th>
<th>CRC</th>
<th>G</th>
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<tbody>
<tr>
<td>4</td>
<td>2</td>
<td>6</td>
<td>16</td>
<td>4</td>
<td>16</td>
<td>160</td>
<td>16</td>
<td>16</td>
</tr>
</tbody>
</table>

- PRBS(PN9)
- R Ramp time for transient response
- SS Start symbol 10
- PR Preamble 011001
- UW Unique word
  - Uplink: E149
  - Downlink: 3D4C
- CI Channel identifier 0000 (TCH)
- SA SACCH All “0”
- G Guard time
Continuous modulated signal patterns select

Downloading the signal pattern file from PC memory card
Contrast of typical ACLR ≤ +5 dBm, Continuous modulation
Auxiliary signal  Input

» Front panel
  – Trigger
    • Synchronization of external frame clock
    • Frame trigger or start trigger is selectable
      – Used at CS receiver test
  – Ref. Clock
    • Synchronization of external baseband reference clock
    • $20 \times$ symbol rate ($20 \times 192 \text{ kbps} = 3,840 \text{ kHz}$)
      – Used at start trigger
    External reference clock input on rear panel (10/13MHz) is also available
Auxiliary signal

Rear panel
- RF Gate
- Sampling Clock
  - Baseband reference clock
    - $20 \times$ symbol rate
      (20× 192 ksp = 3,840 kHz)
- Frame Trigger, Sequence Pulse
  511 frames

Control signal of internal pulse modulator

Digital Output
- AL: RF Gate
- BL: Sampling Clock
- BL: Sequence Pulse

Digital Input/Output
- CL: TCH
- DE: Frame Trigger

Slot1

Auxiliary signal Output
• AWGN for 3GPP(FDD/TDD) and 3GPP2(CDMA2000) standards can be outputted at real time by installing the MU368060A AWGN Unit in the MG3681A Digital Modulation Signal Generator.
• In R&D/production process of base stations(BS) and user equipment(UE), the function is provided as the AWGN source for receiver test.
AWGN test support

- **3GPP(FDD)**
  - At mounting MX368041B W-CDMA Software installed in MU368040A CDMA Modulation Unit together...
    - Wanted signal source (W-CDMA modulation)
    - Interfering signal source (W-CDMA modulation, CW)
    - AWGN source
  - Single unit is performable
  - change < 10 sec

- **3GPP2(CDMA2000)**
  - At mounting MX368033A CDMA2000 1xEV-DO Signal Generation Software installed in MU368030A Universal Modulation Unit together...
    - Wanted signal source (CDMA2000 1xEV-DO modulation)
    - Interfering signal source (CDMA2000 modulation, CW)
    - AWGN source
  - Single unit is performable
  - change < 10 sec
Ioc [dBm] = AWGN level of 3.84MHz (3GPP) or 1.23MHz (3GPP2) bandwidth

To measure for high-accuracy

- By spectrum analyzer
  - Measuring total level (Pt)[dBm]
  - Measuring 3.84MHz or 1.23MHz bandwidth level (Pb)[dBm]
- By power meter
  - Measuring total level (Pm)[dBm]
- Ioc = Pm + (Pb - Pt)

Measuring per frequency

Spectrum analyzer needlessness (accuracy ≤ ±0.6 dB)
Application

- Product outline
- Feature
- Application
- Option

- **3GPP**
  - W-CDMA 3GPP(FDD) 145
  - GSM/EDGE 186

- **3GPP2**
  - CDMA2000 1xEV-DO 188
  - CDMA2000 1X 211

- **ARIB**
  - PHS 226
  - PDC 235

- **TIA**
  - NADC 246
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<th>Wanted signal generator</th>
<th>Interfering signal generator</th>
<th>CW generator</th>
<th>AWGN generator</th>
<th>Others</th>
</tr>
</thead>
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<tr>
<td>6.4</td>
<td>Output power dynamics</td>
<td>MG3681A &lt;br&gt; +MU368040A &lt;br&gt; +MX368041B</td>
<td></td>
<td></td>
<td></td>
<td>Code domain analyzer</td>
</tr>
<tr>
<td>6.4.2</td>
<td>Power control steps</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Spectrum analyzer</td>
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<tr>
<td>6.4.3</td>
<td>Power control dynamic range</td>
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<td></td>
<td></td>
<td></td>
<td>Circulator</td>
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<td>6.6</td>
<td>Transmit intermodulation</td>
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<tr>
<td>7.2</td>
<td>Reference sensitivity level</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7.3</td>
<td>Dynamic range</td>
<td>MG3681A &lt;br&gt; +MU368040A &lt;br&gt; +MX368041B</td>
<td></td>
<td></td>
<td>+MU368060A</td>
<td>MP1201C BERT</td>
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<td>7.4</td>
<td>Adjacent Channel Selectivity (ACS)</td>
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<td>MA1612A</td>
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<tr>
<td>7.5</td>
<td>Blocking characteristics</td>
<td>MG3681A &lt;br&gt; +MU368040A &lt;br&gt; +MX368041B</td>
<td>MG3692A 20GHz or MG3642A 2.08GHz</td>
<td></td>
<td></td>
<td>3GHz Combiner</td>
</tr>
<tr>
<td>7.6</td>
<td>Intermodulation characteristics</td>
<td></td>
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<td></td>
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</tr>
<tr>
<td>7.8</td>
<td>Verification of the internal BER calculation</td>
<td>MG3681A &lt;br&gt; +MU368040A &lt;br&gt; +MX368041B</td>
<td></td>
<td></td>
<td>+MU368060A</td>
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<td>8.2</td>
<td>Demodulation in static propagation conditions</td>
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<td>8.3</td>
<td>Demodulation of DCH in multipath fading conditions</td>
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<tr>
<td>8.4</td>
<td>Demodulation of DCH in moving propagation conditions</td>
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<tr>
<td>8.5</td>
<td>Demodulation of DCH in birth/death propagation conditions</td>
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<tr>
<td>8.6</td>
<td>Verification of the internal BLER calculation</td>
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<td>8.8</td>
<td>RACH performance</td>
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<td>8.8.1</td>
<td>RACH preamble detection in static propagation conditions</td>
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<td>8.8.2</td>
<td>RACH preamble detection in multipath fading case 3</td>
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<tr>
<td>8.8.3</td>
<td>Demodulation of RACH message in static propagation conditions</td>
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</tr>
<tr>
<td>8.8.4</td>
<td>Demodulation of RACH message in multipath fading case 3</td>
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<td>8.9</td>
<td>CPCH performance</td>
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<td>8.9.3</td>
<td>Demodulation of RACH message in static propagation conditions</td>
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<tr>
<td>8.9.4</td>
<td>Demodulation of RACH message in multipath fading case 3</td>
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</tr>
<tr>
<td>8.10</td>
<td>Site Selection Diversity Transmission (SSDT) Mode</td>
<td></td>
<td></td>
<td></td>
<td>+MU368060A</td>
<td></td>
</tr>
</tbody>
</table>
Transmitter test

- Wanted signal generator
  MG3681A
  +MU368040A+MX368041B

- Code domain analyzer
  MS8608A/8609A
  +MX860801B/860901B

- Interfering signal generator
  MG3681A
  +MU368040A+MX368041B
  (+MG3681A-42)

- Spectrum analyzer
  MS8608A/8609A
  +MX860801B/860901B

Connection example

- Power control test
- Transmit intermodulation test

Controller

- Launches the Inner loop power control in the possible state by FTM Factory Test Mode control.
- Launches in the transmitting state by FTM Factory Test Mode control.
Receiver test  Connection example

Interfering signal generator
CW generator
(AWGN generator)
MG3681A
+MU368040A+MX368041B
(+MU368010A+MX368012A)
(+MU368060A)

Wanted signal generator
(+ AWGN generator)
MG3681A
+MU368040A+MX368041B
(+MU368060A)

CW generator
(MG3692A)

- Start trigger
  - Front panel [Clock/Trig] Input
    - 40 ms × n clock
e.g. SFN reset timing of Downlink BCH (2044 frame ×10 ms), BFN timing (4096 frame ×10 ms)

- Reference clock
  Apply only one
  - Front panel [Ref. Clock] Input
    - 3.84 MHz, 2× 3.84 MHz (7.68 MHz), 4× 3.84 MHz (15.36 MHz)
  - Rear panel [10MHz/13MHz Ref] Input
    - 10 MHz, 13 MHz

- Controller
  - Launches UL RMC in the receivable state by FTM Factory Test Mode control.
  - Checks the CRC per demodulated transport block (DTCH) and calculates the BLER.
Timing synchronization  Setup example

- **Start trigger delay**
  - Set the timing to which BS can receive UL RMC

<table>
<thead>
<tr>
<th>Trigger</th>
<th>Delay: 0 chip</th>
</tr>
</thead>
<tbody>
<tr>
<td>38,400 chip</td>
<td>1,024 chip</td>
</tr>
</tbody>
</table>

- **UL DPDCH**
  - SFN reset (SFN=2047)
  - DL DPCH

- **UL DPCCH**
  - SFN reset (SFN=2047)
  - DL DPCH

- **Radio frame**
  - Radio frame
  - Radio frame
  - Radio frame
  - Radio frame

- **10 ms (38,400 chip)  40 ms**
Timing sync. Setup example

- **Setting External Start trigger**
  - Captures/ Synchronizes the Trigger only once

- **Reference clock**:
  - [Ref. Clock] Input applicable case
    - Reference Clock Source: [Ext]
    - Reference Clock / Chip Clock:
      - [1] at 3.84 MHz
      - [2] at 2×3.84 MHz
      - [4] at 4×3.84 MHz
  - [10MHz/13MHz Ref] Input applicable case
    - Reference Clock Source: [Int]

- **Start trigger delay**
  - -38,353.5 ~ +65,536 chip
  - 1/2 chip resolution

- **Trigger recapture/ synchronization**
Scrambling code sync. Setup example

- **Long scrambling code**
  - 38,400 chip (10 ms) length
  - Created from two \((x_n, y)\) binary m-sequences of 25 bit length
  - Applies HPSK modulation at spreading
    - HPSK: QPSK modulation and \(\pi/2\)BPSK modulation alternate per chip timing.
    - Crest factor is lowered without shifting the phase by 180°.

- **Short scrambling code**
  - To mitigate the reception processing of BS when applying interference canceler
  - 256 chip length

- **Set** \(x_n(23) \sim x_n(0)\) **receivable by BS in hexadecimal**
  - \(C_{\text{long},2,n}\) shifts \(C_{\text{long},1,n}\) by 16,777,232 chip
Wanted signal generator Setup example

- UL RMC 12.2 kbps
- UL RMC 64 kbps
- UL RMC 144 kbps
- UL RMC 384 kbps

- Generating the error 1% in DTCH
  » Verification of the internal BER/BLER calculation test
Wanted signal generator  Setup example

- **UL RMC RACH**
  - Preamble
  - Message
    - TB size: 168 bits, 360 bits

- **UL RMC CPCH**
  - TB size: 168 bits, 360 bits
Wanted signal generator Setup example

- UL RMC 12.2 kbps
  - SSDT test
    - Cell ID transmitted by UE: A, B
Wanted signal generator  Setup example

- Set TPC command for Inner loop power control
  - 60 TPC command (60 slots) cycle
    - Power control steps test
      - Transmitter power control step tolerance
        - $[555\ 5555\ 5555\ 5555\ H\ 0101\ 0101\ ...\ 0101\ H\ 0000\ 0000\ 0011\ 1111\ 1111\ 0000\ ...\ 1111\ H\ 0000...\ 0011...1111\ H]$
    - Transmitter aggregated power control step range
      - $[003\ FF00\ 3FF0\ 03FF\ H\ 0000\ 0000\ 0011\ 1111\ 1111\ 0000\ ...\ 1111\ H\ 0000...\ 0011...1111\ H]\ (30\ bits)$
    - Power control dynamic range test
      - $[000\ 0000\ 3FFF\ FFFF\ H\ 0000\ ...\ 0011\ ...\ 1111\ H\ 0000...\ 0011...1111\ H\ (0\ bits, 30\ bits)]$
Interfering signal generator

Setup example

- **W-CDMA**
  - UL RMC 64 kbps
  - Set the scrambling code different from wanted signal
    - [00 0010]
    - in case of Wanted signal: [00 0000]
  - ACP priority filter
Interfering signal generator

**Setup example**

- **Test Model 1**
  - Transmit intermodulation test
  - ACP priority filter

- **GMSK modulation**
  - Blocking characteristics,
  - Intermodulation characteristics test
**AWGN generator**

- **AWGN mixing**
  - C/N = Wanted signal/AWGN
    - Dynamic range test
      - C/N: [-16.8dB]
        
        Wanted: -89.8dBm  
        Noise: -73.0dBm
      - Demodulation in static propagation conditions test
        - C/N: [-19.5dB]
          
          Wanted: -103.5dBm  
          Noise: -84.0dBm
  
  \[
  \text{C/N} = \frac{\text{Wanted Signal}}{\text{Noise}} = \frac{-89.8\text{dBm}}{-73.0\text{dBm}} = 1.22 \approx \text{1.22}
  \]

  \[
  \text{C/N} = \frac{\text{Wanted Signal}}{\text{Noise}} = \frac{-103.5\text{dBm}}{-84.0\text{dBm}} = 1.24 \approx \text{1.24}
  \]

- **AWGN source**
  - Ioc = Total level + Bandwidth level
    
    12.2 kbps: -24.98
    64 kbps: -17.78
    144 kbps: -14.26
    384 kbps: -10
## W-CDMA 3GPP(FDD) UE testing

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<tr>
<th>Section</th>
<th>Test</th>
<th>Wanted signal generator</th>
<th>Interfering signal generator</th>
<th>CW generator</th>
<th>AWGN generator</th>
<th>Others</th>
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<tbody>
<tr>
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<td>Adjacent Channel Selectivity (ACS)</td>
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<td>7.6</td>
<td>Blocking characteristics</td>
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- **Output power dynamics**
- **Inner loop power control in the uplink**
- **Minimum output power**
- **Reference sensitivity level**
- **Maximum input level**
- **HS-PDSCH for 16QAM**
- **Adjacent Channel Selectivity (ACS)**
- **Blocking characteristics**
- **Spurious response**
- **Intermodulation characteristics**

**Tools:**
- MG3681A
- MU368040A
- MX368041B
- BERT
- Combiner
- MP1201C
- MA1612A

**Notes:**
- 3GPP TS 25.101 (Release 5)
- * TS 34.121 (Release 5)
- 6 Transmitter
- 5 Transmitter
- 6 Receiver
**W-CDMA 3GPP(FDD) UE testing**

3GPP TS 25.101 (Release 5) * TS 34.121 (Release 5)

<table>
<thead>
<tr>
<th>Performance requirement</th>
<th>7</th>
<th>Performance requirements</th>
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<td>Performance requirement (HSDPA)</td>
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<thead>
<tr>
<th>Section</th>
<th>Test</th>
<th>Wanted signal generator</th>
<th>Interfering signal generator</th>
<th>CW generator</th>
<th>AWGN generator</th>
<th>Others</th>
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<td>Demodulation in static propagation conditions</td>
<td>MG3681A+MU368040A</td>
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<td>8.3</td>
<td>Demodulation of DCH in multi-path fading propagation conditions</td>
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<td>Demodulation of DCH in moving propagation conditions</td>
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<td>Demodulation of DCH in birth-death propagation conditions</td>
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<td>8.6</td>
<td>Demodulation of DCH in downlink Transmit diversity modes</td>
<td>MG3681A x2</td>
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<td>MG3681A+MU368060A</td>
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<td>8.6.1</td>
<td>Demodulation of DCH in open-loop transmit diversity modes</td>
<td>MG3681A+MU368040A</td>
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<td>8.9</td>
<td>Downlink compressed mode</td>
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<td>MA1612A 3GHz Combiner</td>
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<td>8.10</td>
<td>Blind transport format detection</td>
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<td>Demodulation of Paging Channel</td>
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<td>Demodulation of HS-DSCH (FRC)</td>
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<td>MA1612A 3GHz Combiner</td>
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<td>Single Link performance</td>
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<td>9.3</td>
<td>Reporting of Channel Quality Indicator (CQI)</td>
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</table>
Transmitter test  Connection example

- Controller
  - Launches the Inner loop power control in the possible state by FTM Factory Test Mode control.

Wanted signal generator
MG3681A
+MU368040A+MX368041B

(Slot) Power meter
MS8608A/8609A
+MX860801B/860901B
Receiver test  Connection example

Interfering signal generator
CW generator
AWGN generator
MG3681A
+MU368040A+MX368041B
(+MU368010A+MX368012A)
+MU368060A

Wanted signal generator
MG3681A
+MU368040A+MX368041B
(+MX368041B-11)

CW generator
(MG3692A)

Controller

- Launches DL RMC in receivable state by FTM Factory Test Mode control.
- Checks the CRC per demodulated transport block (DTCH) and calculates the BLER.
Scrambling code sync.  Setup example

• **Long scrambling code**
  – Created from Gold sequences of 18 bit length
    » Applies QPSK modulation at spreading
• **Set the Scrambling code receivable by UE in hexadecimal**
  » $0 \sim 3FFFF \ (2^{18} - 1)$
    – Primary scrambling code: $16 \times (8 \times j + k) = 0 \sim 01FF0$
    – Secondary scrambling code: $16 \times (8 \times j + k) + (1 \sim 15)$
    » 512 codes $(i = 0 \sim 511)$
      – 64 Scrambling code group $j = 0 \sim 63$
      – 8 Primary scrambling code $k = 0 \sim 7$
Applicable codes for SCH spreading modulation

- When scrambling code group (j) was changed...

Set in reference to 3GPP TS 25.213 5.2.3.2

Table 4: Allocation of SSCs for secondary SCH

Due to the pair with SSC Secondary Synchronisation Code allocation for S-SCH.
### For reference: 3GPP TS 25.213 (Release 5) Table 4

#### Group 0: Default setting

<table>
<thead>
<tr>
<th>Scrambling Code Group</th>
<th>slot number</th>
<th>Scrambling Code Group</th>
<th>slot number</th>
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<tbody>
<tr>
<td>Group 0</td>
<td>#0 #1 #2 #3 #4 #5 #6 #7 #8 #9 #10 #11 #12 #13 #14</td>
<td>Group 32</td>
<td>#0 #1 #2 #3 #4 #5 #6 #7 #8 #9 #10 #11 #12 #13 #14</td>
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<tr>
<td>Group 1</td>
<td>#2 #4 #5</td>
<td>Group 33</td>
<td>#2 #4 #5</td>
</tr>
<tr>
<td>Group 2</td>
<td>#2 #4 #5</td>
<td>Group 34</td>
<td>#0 #1 #2 #3 #4 #5 #6 #7 #8 #9 #10 #11 #12 #13 #14</td>
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<td>Group 3</td>
<td>#0 #1 #2 #3 #4 #5 #6 #7 #8 #9 #10 #11 #12 #13 #14</td>
<td>Group 35</td>
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<td>Group 4</td>
<td>#0 #1 #2 #3 #4 #5 #6 #7 #8 #9 #10 #11 #12 #13 #14</td>
<td>Group 36</td>
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<td>Group 42</td>
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<td>Group 63</td>
<td>#0 #1 #2 #3 #4 #5 #6 #7 #8 #9 #10 #11 #12 #13 #14</td>
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</tbody>
</table>
Wanted signal generator Setup example

- DL RMC 12.2 kbps
  » Receiver test

- DL RMC 12.2 kbps
  » Maximum input level (DPCH), Performance requirement test
    - OCNS multiplexing
Wanted signal generator Setup example

- DL RMC 12.2 kbps
- DL RMC 64 kbps
- DL RMC 144 kbps
- DL RMC 384 kbps
  - Performance requirement test

- DL RMC 12.2 kbps DPCCH with 4 pilot bits as phase reference
  - Demodulation of DCH in multi-path fading propagation conditions (Case 7) Test 21~25 test
Wanted signal generator Setup example

- **DL compressed mode**
  - Downlink compressed mode test
    - Test 1,2: Reference pattern 1 Set 1
      - DL SF/2 (Spreading factor reduction)
    - Test 3,4: Reference pattern 1 Set 2
      - DL Puncturing
      - Reference pattern 2 Set 1
      - Reference pattern 2 Set 2
        - DL SF/2 (Spreading factor reduction)
      - Reference pattern 2 Set 3
        - DL Puncturing

- **DL RMC BTFD**
  - Blind transport format detection test
    - Test 1,4: 12.2 kbps (Rate 1)
    - Test 2,5: 7.95 kbps (Rate 2)
    - Test 3,6: 1.95 kbps (Rate 3)

- **DL PCH**
  - Demodulation of Paging Channel test
Interfering signal generator

Setup example

- ACP priority filter
  - OCNS multiplexing
AWGN generator  Setup example

- AWGN source
  \[ I_{oc} = \text{Total level} + \text{Bandwidth level} \]

Freq. 2112.500 000 00 MHz
Level - 57.81 dBm
Open-loop TX Diversity mode test Connection example

- Start trigger
  - Front panel [Clock/Trig] Input
- Reference clock
  - Rear panel [10MHz Buff] Output
  - Rear panel [10MHz/13MHz Ref] Input
- Controller
  - Launches DL RMC in receivable state by FTM Factory Test Mode control.
  - Checks the CRC per demodulated transport block (DTCH) and calculates the BLER.
• **DL RMC 12.2 kbps**
  > Demodulation of DCH in open-loop Transmit diversity mode test
  > - Antenna 1
  > - Antenna 2

• **Setting External Start trigger**
  > Captures/ Synchronizes the Trigger only once

• **Trigger recapture/ synchronization**
Wanted signal generator  Setup example

- Set TPC command for Inner loop power control
  - 60 TPC command (60 slots) cycle
    - Step A (1 dB step \{0\})
      - \([82A BE82 ABE8 2ABE]_H\)
    - Step B (1 dB step \{0,0,0,0,+1\})
      - \([FFFF FFFF FFFF FFFF]_H\)
    - Step C (1 dB step \{0,0,0,0,-1\})
      - \([000 0000 0000 0000]_H\)
    - Step D (1 dB step \{+1\})
      - \([FFFF FFFF FFFF FFFF]_H\)
    - Step E (1 dB step \{-1\})
      - \([000 0000 0000 0000]_H\)
    - Step F (1 dB step \{+1\})
      - \([FFFF FFFF FFFF FFFF]_H\)
    - Step G (2 dB step \{-1\})
      - \([000 0000 0000 0000]_H\)
  - Minimum output power test
    - Minimum output power test
      - \([000 0000 0000 0000]_H\)
Wanted signal generator
MG3681A
+MU368040A+MX368041B
+MX368041B-11

HSDPA demodulation test

Connection example

Signal analyzer
(MS8600/MS2680)

Table C.8: Downlink physical channels for HSDPA receiver testing for Single Link performance.

<table>
<thead>
<tr>
<th>Physical Channel</th>
<th>Parameter</th>
<th>Value</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>P-CPICH</td>
<td>P-CPICH_Ec/lor</td>
<td>-10dB</td>
<td>Mean power level is shared with SCH.</td>
</tr>
<tr>
<td>P-CCPCH</td>
<td>P-CCPCH_Ec/lor</td>
<td>-12dB</td>
<td>Mean power level is shared with P-CPICH – SCH includes P- and S-SCH, with power split between both. P-SCH code is S_dl,0 as per TS25.213 S-SCH pattern is scrambling code group 0.</td>
</tr>
<tr>
<td>SCH</td>
<td>SCH_Ec/lor</td>
<td>-12dB</td>
<td>Mean power level is shared with P-CPICH – SCH includes P- and S-SCH, with power split between both. P-SCH code is S_dl,0 as per TS25.213 S-SCH pattern is scrambling code group 0.</td>
</tr>
<tr>
<td>DPCH</td>
<td>DPCH_Ec/lor</td>
<td>Test-specific</td>
<td>12.2 kbps DL reference measurement channel as defined in Annex A.2.1</td>
</tr>
<tr>
<td>HS-SCCH_1</td>
<td>HS-SCCH_Ec/lor</td>
<td>Test-specific</td>
<td>Specifies fraction of Node-B radiated power transmitted when TTI is active (i.e. due to minimum inter-TTI interval).</td>
</tr>
<tr>
<td>HS-SCCH_2</td>
<td>HS-SCCH_Ec/lor</td>
<td>DTXd</td>
<td>No signalling scheduled, or power radiated, on this HS-SCCH, but signalled to the UE as present.</td>
</tr>
<tr>
<td>HS-SCCH_3</td>
<td>HS-SCCH_Ec/lor</td>
<td>DTXd</td>
<td>As HS-SCCH_2.</td>
</tr>
<tr>
<td>HS-SCCH_4</td>
<td>HS-SCCH_Ec/lor</td>
<td>DTXd</td>
<td>As HS-SCCH_2.</td>
</tr>
<tr>
<td>HS-PDSCH</td>
<td>HS-PDSCH_Ec/lor</td>
<td>Test-specific</td>
<td>Necessary power so that total transmit power spectral density of Node B (Ior) adds to one. OCNS interference consists of 6 dedicated data channels as specified in table C.12.</td>
</tr>
</tbody>
</table>

OCNS

Necessary power so that total transmit power spectral density of Node B (Ior) adds to one. OCNS interference consists of 6 dedicated data channels as specified in table C.12.
HSDPA Baseband test

Connection example

Wanted signal generator
MG3681A
+MG3681A-11
+MU368040A+MX368041B
+MX368041B-11

Inf. Bit checking

- BLER test
- CRC checking

- PN15
  - Reset to initial value per subframe
  - All subframes are the same data

Inf. Bit Payload: 4064
CRC Addition: 4664
Code Block Segmentation: 4688
Turbo-Encoding (R=1/3): 14064
1st Rate Matching: 9600
RV Selection: 7680
Physical Channel Segmentation: 1920

Figure A.17: Coding rate for Fixed reference Channel H-Set 3 (16QAM)
HSDPA CQI test  

Connection example

- Controller
  - Launches DL FRC in receivable state by FTM Factory Test Mode control.
  - Monitors CQI Channel Quality Indicator on UL HS-DPCCH and calculates BLER of DL HS-PDSCH.

Wanted signal generator
MG3681A
+MU368040A+MX368041B
+MX368041B-11

AWGN generator
MG3681A
+MU368060A

Controller

(AWGN generator)
MG3681A
+MU368060A

(Terminator)
(MP752A)

(Combiner)
(MA1612A)
Wanted signal generator Setup example

- DL FRC
  - H-Set 1
    - 16QAM
    - QPSK
  - H-Set 2
    - 16QAM
    - QPSK
  - H-Set 3
    - 16QAM
    - QPSK
  - H-Set 4
    - QPSK
  - H-Set 5
    - QPSK
- ALC Off
RF/IF components test

Connection example

Signal source
MG3681A
+MU368040A+MX368041B

Signal analyzer
(MS8600/MS2680)

Reference clock

Spurious elimination filter
(MA2512A)

- Unwanted signals can be eliminated by connecting the filter if the spurious of signal source obstructs the evaluation.

Spurious of MG3681A
- 660 MHz (IF leakage)
- +660 MHz offset (Local leakage)
- 2×freq./3×freq. (2nd/3rd harmonics)
Downlink signal

BS transmitter test
- Test Model 1
  - Single carrier
  - multi-carrier (2 carriers)
- Test Model 2
- Test Model 3
- Test Model 4
- Test Model 5
  - Single carrier
  - multi-carrier (2 carriers)

- ACP priority filter
  - Spectrum emission mask
  - ACLR
  - Spectrum emissions
• Test Model 1
  » 64 DPCH
    – Single carrier
  – 2 carriers
• **Test Model 5**
  » 30 DPCH + 8 HS-PDSCH
    - Single carrier
  
  - 2 carriers
Downlink signal

Setup example

UE receiver test
- **DL RMC 12.2 kbps**
  - for RX test
  - for Performance test
- **DL RMC 64 kbps**
- **DL RMC 144 kbps**
- **DL RMC 384 kbps**
Uplink signal Setup example

UE transmitter test
BS receiver test
- UL RMC 12.2 kbps
- UL RMC 64 kbps
- UL RMC 144 kbps
- UL RMC 384 kbps

- ACP priority filter
  Transmitter test
  » Spectrum emission mask
  » ACLR
  » Spectrum emissions
UL RMC

- 12.2 kbps
- 384 kbps

Table A.1: Reference measurement channels for UL DCH

<table>
<thead>
<tr>
<th>Parameter</th>
<th>DCH for DTCH / DCH for DCCH</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>DPDCCH</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Information bit rate</td>
<td>12.2/2.4</td>
<td>64/2.4</td>
</tr>
<tr>
<td>Physical channel</td>
<td>60/15</td>
<td>240/15</td>
</tr>
<tr>
<td>Spreading factor</td>
<td>84</td>
<td>16</td>
</tr>
<tr>
<td>Repetition rate</td>
<td>22/22</td>
<td>19/19</td>
</tr>
<tr>
<td>Interleaving</td>
<td>20</td>
<td>40</td>
</tr>
<tr>
<td>Number of DPDCCHs</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>DPCCCH</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dedicated pilot</td>
<td>8</td>
<td>bit/slot</td>
</tr>
<tr>
<td>Power control</td>
<td>2</td>
<td>bit/slot</td>
</tr>
<tr>
<td>TFCl</td>
<td>2</td>
<td>bit/slot</td>
</tr>
<tr>
<td>FBI</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>Spreading factor</td>
<td>256</td>
<td></td>
</tr>
<tr>
<td>Power ratio of DPCCCH/DPDCCH</td>
<td>-5.46</td>
<td>-9.54</td>
</tr>
<tr>
<td>Amplitude ratio of DPCCCH/DPDCCH</td>
<td>0.7333</td>
<td>0.5333</td>
</tr>
</tbody>
</table>

Note: Combination of TFCl bit of 0 bit/slot and FBI bit of 2 bit/slot is applied in test of Site Selection Diversity Transmission specified in 8.10.
Peak Clipping of modulation signal  Setup example

- Useful for the evaluation of crest factor (CCDF)
  - Limiting the peak level of I/Q amplitude before FIR filtering
    - I or Q RMS level
      + 0 ~ 20 dB, 0.1 dB resolution
    - Measure CCDF of output signal (after FIR filtering) by signal analyzer (MS8608A/09A), and adjust the level to limit.
    - ACLR of output signals is not deteriorated because of no distortion caused by clipping.
      - Extreme clipping deteriorates waveform quality.
  - Scalar clipping
    - Limiting I or Q amplitude level
Multi-carrier signal source

- Test model 1 (64 DPCH)
  - Scrambling code
    - 00,10,20,30 [HEX]
  - Typical ACLR [dB/3.84MHz]
    - Lower/Upper
      - 5MHz offset: -62.6/-62.4
      - 10MHz offset: -63.3/-64.4
      - 15MHz offset: -63.2/-64.4
GSM/EDGE
RF/IF components test  Connection example

Signal source
MG3681A
+MU368010A+MX368012A
or
+MU368030A+MX368031A

Reference clock

Signal analyzer
(MS8600/MS2680)
Downlink/Uplink signal Setup example

- **MX368012A**
  - GMSK modulation
    - Data + GP Guard period (8.25 symbol)
  - Burst format
  - Normal burst format for TCH
  - Access burst format for RACH
  - Continuous modulation format

- **MX368031A**
  - 8PSK modulation
    - Continuous modulation format
  - GMSK modulation
    - Continuous modulation format
# CDMA2000 1xEV-DO 3GPP2 AN Access Network testing

3GPP2 C.S0032 -0 v2.0

3.1.1 Receiver Minimum Standards
3.1.1 Transmitter Minimum Standards

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<th>Interfering signal generator</th>
<th>CW generator</th>
<th>AWGN generator</th>
<th>Others</th>
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<td></td>
<td>+MU368060A</td>
<td>+MU368040A</td>
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<tr>
<td>3.1.1.4.1</td>
<td>Receiver Sensitivity</td>
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<td>Receiver Dynamic Range</td>
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<td></td>
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<td>+MU368060A</td>
<td>+MU368040A</td>
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<tr>
<td>3.1.1.4.3</td>
<td>Single Tone Desensitization</td>
<td>MG3681A or 3GHz</td>
<td>MG3642A 2.08GHz</td>
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<td>3.1.1.4.4</td>
<td>Intermodulation Spurious Response Attenuation</td>
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<td>MG3681A 2.08GHz</td>
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<td></td>
<td></td>
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<tr>
<td>3.1.1.4.5</td>
<td>Adjacent Channel Selectivity</td>
<td>MG3681A +MU368030A +MX368033A</td>
<td></td>
<td></td>
<td></td>
<td>MA1612A 3GHz Combiner</td>
</tr>
<tr>
<td>3.1.1.4.6</td>
<td>Receiver Blocking Characteristics</td>
<td>MG3681A 3GHz</td>
<td>MG3692A 20GHz or MG3642A 2.08GHz</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>3.1.1.6</td>
<td>Received Signal Quality Indicator (RSQI)</td>
<td></td>
<td></td>
<td></td>
<td>+MU368060A</td>
<td>+MU368040A</td>
</tr>
<tr>
<td>3.1.2.4.3</td>
<td>Inter-Sector Transmitter Intermodulation</td>
<td>MG3681A +MU368030A +MX368031A (+MG3681A-42)</td>
<td></td>
<td></td>
<td></td>
<td>Spectrum analyzer</td>
</tr>
</tbody>
</table>

Discover What’s Possible™

Slide 188
MG3681A-E-I-1
Inter-Sector Transmitter Intermodulation test
Connection example

- Controller
  - Launches in the transmitting state by FTM Factory Test Mode control.

Interfering signal generator
MG3681A
+MU368030A+MX368031A
(+MG3681A-42)

Spectrum analyzer
MS8608A/8609A
+MX860804A/860904A

Controller


**Receiver test**  
**Connection example**

Interfering signal generator  
CW generator  
(AWGN generator)  
MG3681A  
+MU368030A+MX368031A  
(+MU368060A)

Wanted signal generator  
(+ AWGN generator)  
MG3681A  
+MU368030A+MX368033A  
(+MU368060A+MU368040A)

CW generator  
(MG3692A)

- Start trigger  
  - Front panel [Trigger] Input  
    - Apply only one  
      - 26.66... ms clock (Short sequence rollover)  
      - 426.66... ms clock (Control Channel Cycle)  
      - 2 sec (Even second time mark)

- Reference clock  
  - Front panel [Ref. Clock] Input  
    - 8 × 1.2288 MHz (9.8304 MHz)  
  - Rear panel [10MHz/13MHz Ref] Input  
    - 10 MHz, 13 MHz

- Controller  
  - Launches Reverse Traffic channel in receivable state by FTM Factory Test Mode control.  
  - Checks the CRC per demodulated Traffic channel packet and calculates the PER.
Timing synchronization  Setup example

- **Start trigger delay**
  - Set the timing to which AN can receive Reverse Traffic channel

Reverse Traffic Channel
- Pilot & RRI Channel
- Data Channel
- DRC Channel
- ACK Channel

Start trigger

Forward Traffic Channel

Delay: 1.125 ~ 2,097,153 chip

$1.66\ldots\text{ms (2,048 chip)}$

$26.66\ldots\text{ms}$
Timing sync.  Setup example

- **Setting External Start trigger**
  - Captures/ Synchronizes the Trigger only once
- **Reference clock:**
  - [Ref. Clock] Input applicable case
    - Reference Clock : [Ext(TTL)]
      - 8× 1.2288 MHz (9.8304 MHz)
    - [10MHz/13MHz Ref] Input applicable case
      - Reference Clock : [Int]
- **Start trigger delay**
  - 0 ~ 16,777,215 /8 chip
    - 1/8 chip resolution
  - Delay from Trigger
    - 9/8 chip
      - 1.125 ~ 2,097,153 chip

- **Trigger recapture/ synchronization**

![Image](image_url)
Long Code Mask sync.

- **Reverse Traffic Channel Long Code Mask**
  - 42-bit $M_{\text{IRTCMAC}}$
    - Derived from $M_{\text{IRTCMAC}}$
      - $M_{\text{MQRTCMAC}}[k] = M_{\text{IRTCMAC}}[k-1], \text{ for } k = 1,\ldots,41$
      - $M_{\text{MQRTCMAC}}[0] = M_{\text{IRTCMAC}}[0] \oplus M_{\text{IRTCMAC}}[1] \oplus M_{\text{IRTCMAC}}[2] \oplus M_{\text{IRTCMAC}}[4] \oplus M_{\text{IRTCMAC}}[5] \oplus M_{\text{IRTCMAC}}[6] \oplus M_{\text{IRTCMAC}}[9] \oplus M_{\text{IRTCMAC}}[15] \oplus M_{\text{IRTCMAC}}[16] \oplus M_{\text{IRTCMAC}}[17] \oplus M_{\text{IRTCMAC}}[18] \oplus M_{\text{IRTCMAC}}[20] \oplus M_{\text{IRTCMAC}}[21] \oplus M_{\text{IRTCMAC}}[24] \oplus M_{\text{IRTCMAC}}[25] \oplus M_{\text{IRTCMAC}}[26] \oplus M_{\text{IRTCMAC}}[30] \oplus M_{\text{IRTCMAC}}[32] \oplus M_{\text{IRTCMAC}}[34] \oplus M_{\text{IRTCMAC}}[41]$
      - $\oplus$: XOR
  - 42-bit $M_{\text{MQRTCMAC}}$

- **Setting AN**
  - $M_{\text{IRTCMAC}} = 3\text{FF00000000}$
  - $M_{\text{MQRTCMAC}} = 3\text{FE00000001}$
Wanted signal generator Setup example

- **Reverse Traffic Channel**
  - Data Rate
    - 9.6 kbps
    - 19.2 kbps
    - 38.4 kbps
    - 76.8 kbps
    - 153.6 kbps
Interfering signal generator

**Setup example**

- **HRPD signal**
  - CDMA2000 1xEV-DO
  - Reverse Traffic Channel
    - Adjacent Channel Selectivity test

- **Sector 2 (Interferer)**
  - Inter-Sector Transmitter
  - Intermodulation test

---

**Image Description**

The image shows a setup example for an interfering signal generator. The frequency is set to 900.000 MHz with a level of 3.00 dBm. The system configuration includes options for different modes and patterns. The setup is used for testing adjacent channel selectivity and intermodulation in a CDMA2000 1xEV-DO network.
**AWGN generator**

**Setup example**

- **AWGN mixing**
  - C/N = Wanted signal/AWGN
    - **Dynamic range test**
      - C/N: [1.2dB]
        - Wanted -63.8dBm Noise -65.0dBm
    - **RSQI test**
      - C/N: [1.0dB]
        - Wanted -83.0dBm Noise -84.0dBm
        - (Data rate: 153.6 kbps, Data Eb/Nt: 8 dB, DataChannelGain: 18.5 dB)
        - $I_{oc} = N_t \times 1.23 \times 10^6 \times \text{ChannelGain}$

- **AWGN source**
  - $I_{oc} = \text{Total level} + \text{Bandwidth level}$
### 3GPP2 C.S0033 -0 v2.0

#### 3.1.1 Receiver Minimum Standards

<table>
<thead>
<tr>
<th>Section</th>
<th>Test</th>
<th>Wanted signal generator</th>
<th>Interfering signal generator</th>
<th>CW generator</th>
<th>AWGN generator</th>
<th>Others</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.1.1.2.1</td>
<td>Demodulation of Forward Traffic Channel in AWGN</td>
<td></td>
<td></td>
<td></td>
<td>+MU368060A</td>
<td>MG3681A+MU368040A</td>
</tr>
<tr>
<td>3.1.1.2.2</td>
<td>Demodulation of Forward Traffic Channel in Multipath Fading Channel</td>
<td></td>
<td></td>
<td></td>
<td>MG3681A</td>
<td>Channel simulator, Combiner</td>
</tr>
<tr>
<td>3.1.1.3.1</td>
<td>Receiver Sensitivity and Dynamic Range</td>
<td>MG3681A</td>
<td></td>
<td>MG3642A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.1.1.3.2</td>
<td>Single Tone Desensitization</td>
<td>MG3681A</td>
<td></td>
<td>MG3642A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.1.1.3.3</td>
<td>Intermodulation Spurious Response Attenuation</td>
<td>MG3681A</td>
<td></td>
<td>MG3642A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.1.1.3.4</td>
<td>Adjacent Channel Selectivity</td>
<td>MG3681A</td>
<td></td>
<td>MG3692A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.1.1.4.5</td>
<td>Receiver Blocking Characteristics</td>
<td>MG3681A</td>
<td></td>
<td>MG3692A</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Receiver test  Connection example

Interfering signal generator
CW generator
(AWGN generator)
MG3681A
+MU368030A+MX368031A
(+MU368060A)

Wanted signal generator
(AWGN generator)
MG3681A
+MU368030A+MX368033A
(+MU368060A+MU368040A)

CW generator
(MG3692A)

Combiner
(MA1612A)

Controller
PER calculation

- Controller
  - Launches Forward Traffic channel in receivable state by FTM Factory Test Mode control.
  - Checks the CRC per demodulated Traffic channel packet and calculates the PER.
Wanted signal generator Setup example

- **Forward Traffic Channel**

  Data Rate  | Slots per Physical Layer Packet
  --- | ---
  38.4 kbps | 16
  76.8 kbps | 8
  153.6 kbps | 4
  307.2 kbps | 2
  614.4 kbps | 1
  307.2 kbps | 4
  614.4 kbps | 2
  1,228.8 kbps | 1
  921.6 kbps | 2
  1,843.2 kbps | 1
  1,228.8 kbps | 2
  2,457.6 kbps | 1
Interfering signal generator

Setup example

- **HRPD signal**
  - CDMA2000 1xEV-DO Forward Traffic Channel

or

- **CDMA signal**
  - CDMA2000 1X Forward Traffic Channel
AWGN generator

Setup example

- **AWGN mixing**
  - $C/N = \frac{\text{Wanted signal}}{\text{AWGN}}$
  - Demodulation of FTC in AWGN test
  - $C/N: \text{I}_o/\text{I}_{oc}$

- **AWGN source**
  - $\text{I}_{oc} = \text{Total level} + \text{Bandwidth level}$

[Image of AWGN Setup example]
**RF/IF components test**  
**Connection example**

- **Signal source**
  - MG3681A
  - MU368030A+MX368033A
  - or MX368031A

- **Signal analyzer**
  - (MS8600/MS2680)

- **Reference clock**

- **Frame trigger**
  - Required when performing modulation analysis of Reverse signal by MS8608A/8609A
    - Because, it cannot catch Pilot Channel when DataChannelGain is high.
  - Rear panel A4[Frame Trigger] or B2[Sequence Pulse] Output
    - To MS8608A/8609A rear panel [Trigger] Input
    - 26.66... ms clock

---

<table>
<thead>
<tr>
<th>Rate (kbps)</th>
<th>DataChannelGain (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.6</td>
<td>3.75</td>
</tr>
<tr>
<td>19.2</td>
<td>6.75</td>
</tr>
<tr>
<td>38.4</td>
<td>9.75</td>
</tr>
<tr>
<td>76.8</td>
<td>13.25</td>
</tr>
<tr>
<td>153.6</td>
<td>18.50</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Field</th>
<th>Value (Decimal)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRCLength</td>
<td>0 (1 slot)</td>
</tr>
<tr>
<td>DRCChannelGain</td>
<td>6 (3 dB)</td>
</tr>
<tr>
<td>ACKChannelGain</td>
<td>6 (3 dB)</td>
</tr>
</tbody>
</table>
Forward signal Setup example

AN transmitter test
AT receiver test

- **MX368033A**
  - Active Slot: 8,4,3,2,1 carrier
    - 2,457.6 kbps, 16QAM
  - Idle Slot: 8,4,3,2,1 carrier
    - Burst signal

- **MX368031A**
  - Active Slot: single carrier
    - 2,457.6 kbps, 16QAM
  - Idle Slot: single carrier
    - Burst signal
CCDF

- **Active slot**
  - Single carrier
  - 2 carriers
  - 8 carriers
CCDF

- **Idle slot**
  - Single carrier
    - Mean power of the ensemble average $\approx$ Mean power of the Pilot/MAC channel ensemble average - 6.6 dB
Reverse signal Setup example

AT transmitter test
AN receiver test

- **MX368033A**
  - 9.6 kbps
  - 153.6 kbps
- **MX368031A**
  - 9.6 kbps
  - 153.6 kbps
Investigation of Reverse signal (9.6 / 153.6 kbps)

- **I**
  - Pilot Channel 0 dB
  - ACK Channel 3 dB

- **Q**
  - DRC Channel 3 dB
  - Data Channel 3.75 dB (9.6 kbps)
    - 6.75 dB (19.2 kbps)
    - 9.75 dB (38.4 kbps)
    - 13.25 dB (76.8 kbps)
    - 18.5 dB (153.6 kbps)
9.6 kbps Constellation

- **I**
  - Pilot Channel 1
  - ACK Channel $\approx 1.4$
    - Half-slot transmission

- **Q**
  - DRC Channel $\approx 1.4$
  - Data Channel $\approx 1.5$

The right figure which plotted IQ inclines 45° in Spreading, and rotates 90°.
153.6 kbps Constellation

- **I**
  - Pilot Channel 1
  - ACK Channel \( \approx 1.4 \)
  - Half-slot transmission

- **Q**
  - DRC Channel \( \approx 1.4 \)
  - Data Channel \( \approx 8.4 \)

The right figure which plotted IQ inclines 45° in Spreading, and rotates 90°.
CCDF

- On the result of Constellation, 9.6 kbp side tends to generate the peak.

- Although specified that $\rho$ test is 9.6 kbps and Spurious test is 153.6 kbps in 3GPP2, it is necessary to consider also 9.6 kbps which the peak tends to generate.
## CDMA2000 1X 3GPP2 BS testing

### 3GPP2 C.S0010 -B v1

3. Receiver Minimum Standards
4. Transmitter Minimum Standards

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<th>Interfering signal generator</th>
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<th>AWGN generator</th>
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<td></td>
<td></td>
<td></td>
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<td>3.5.2</td>
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<td>MG3681A or 3GHz</td>
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<td>3.5.3</td>
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<td>3.5.4</td>
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<tr>
<td>3.5.5</td>
<td>Adjacent Channel Selectivity</td>
<td>MG3681A + MU368030A + MX368031A</td>
<td></td>
<td>MG3692A 200GHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.5.6</td>
<td>Receiver Blocking</td>
<td>MG3681A or 3GHz</td>
<td></td>
<td>MG3692A 200GHz or MG3642A 2.08GHz</td>
<td></td>
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</tr>
<tr>
<td>3.7</td>
<td>Received Signal Quality Indicator (RSQI)</td>
<td></td>
<td></td>
<td></td>
<td>MG3681A or 3GHz</td>
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</tr>
<tr>
<td>4.4.3</td>
<td>Inter-Base Station Transmitter Intermodulation</td>
<td></td>
<td></td>
<td></td>
<td>MG3681A or 3GHz</td>
<td>Spectrum analyzer Circulator</td>
</tr>
</tbody>
</table>

---

Discover What’s Possible™

Anritsu

Slide 211

MG3681A-E-I-1
Inter-Base Station Transmitter Intermodulation test  Connection example

- Interfering signal generator
  MG3681A
  +MU368030A+MX368031A
  (+MG3681A-42)

- Spectrum analyzer
  MS8608A/8609A
  +MX860803A/860903A

- Controller
  - Launches in the transmitting state by FTM Factory Test Mode control.
Interfering signal generator
CW generator
AWGN generator
MG3681A
+MU368030A+MX368031A
+MU368060A

Wanted signal generator
MG3681A
+MU368030A+MX368031A

CW generator
(MG3692A)

- Start trigger
  - Front panel [Trigger] Input
    - Apply only one
    - 20 ms frame clock
    - 80 ms clock (Alignment of frame clock and zero PN offset 26.67 ms clock)
    - 2 sec clock (Even second time mark)
  - Reference clock
    - Apply only one
    - Front panel [Ref. Clock] Input
      - 8× 1.2288 MHz (9.8304 MHz)
    - Rear panel [10MHz/13MHz Ref] Input
      - 10 MHz, 13 MHz
- Controller
  - Launches Reverse Traffic channel in receivable state by FTM Factory Test Mode control.
  - Checks the CRC per demodulated Traffic channel frame and calculates the FER.
Timing synchronization  Setup example

- **Start trigger delay**
  - Set the timing to which MS can receive Reverse Traffic channel

  Reverse Traffic Channel
  - Pilot Channel
  - Dedicated Control Channel
  - Fundamental Channel
  - Supplemental Channel

  Forward Traffic Channel

  **Pilot PN Sequence**

  **Frame**

  \[26.666... \text{ms}\]

  **Delay: 1.125 \sim 2,097,153 \text{chip}**

  **Start trigger**

  **20 \text{ms} (24,576 \text{chip})**

  **80 \text{ms}**
Timing sync. Setup example

- **Setting External Start trigger**
  - Captures/ Synchronizes the Trigger only once

- **Reference clock**
  - [Ref. Clock] Input applicable case
    - Reference Clock : [Ext(TTL)]
      - $8 \times 1.2288 \text{ MHz } (9.8304 \text{ MHz})$
    - [10MHz/13MHz Ref] Input applicable case
      - Reference Clock : [Int]

- **Start trigger delay**
  - $0 \sim 16,777,215 /8 \text{ chip}$
    - 1/8 chip resolution
  - Delay from Trigger
    - $+9/8 \text{ chip}$
    - $1.125 \sim 2,097,153 \text{ chip}$
Long Code Mask sync.

- Reverse Traffic Channel Long Code Mask
  » 42-bit PN sequence

- Setting BS
  » 00000000000
Wanted signal generator Setup example

- **Reverse Traffic Channel**

<table>
<thead>
<tr>
<th>Test Mode</th>
<th>Forward Traffic Channel Radio Configuration</th>
<th>Reverse Traffic Channel Radio Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
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<tr>
<td>4</td>
<td>4</td>
<td>3</td>
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<td>5</td>
<td>5</td>
<td>4</td>
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<tr>
<td>6</td>
<td>6</td>
<td>5</td>
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<tr>
<td>7</td>
<td>7</td>
<td>5</td>
</tr>
<tr>
<td>8</td>
<td>8</td>
<td>6</td>
</tr>
<tr>
<td>9</td>
<td>9</td>
<td>6</td>
</tr>
</tbody>
</table>
Interfering signal generator

Setup example

- **RC 3 signal**
  - Adjacent Channel Selectivity test

- **External Base Station**
  - Inter-Sector Transmitter Intermodulation test
AWGN generator Setup example

- **AWGN source**
  - $I_{oc} = \text{Total level} + \text{Bandwidth level}$
RF/IF components test

**Signal source**
- MG3681A
- +MU368030A+MX368031A
- or
- +MU368040A+MX368042A

**Reference clock**

**Signal analyzer**
- (MS8600/MS2680)

Connection example
Forward signal Setup example

BS transmitter test
MS receiver test

- **MX368031A**
  - RC 1/2
  - RC 3/4/5

- **MX368042A**
  - RC 1
  - RC 2

<table>
<thead>
<tr>
<th>Channel Type</th>
<th>Relative Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pilot</td>
<td>0.2 of total power (linear)</td>
</tr>
<tr>
<td>Sync+Paging+Traffic</td>
<td>Remainder (0.8) of total power (linear)</td>
</tr>
<tr>
<td>Sync</td>
<td>3 dB less than one Fundamental Traffic Channel; always 1/8 rate</td>
</tr>
<tr>
<td>Paging</td>
<td>3 dB greater than one Fundamental Traffic Channel; full rate only</td>
</tr>
<tr>
<td>Traffic</td>
<td>Equal power in each Fundamental Traffic Channel; full rate only</td>
</tr>
</tbody>
</table>

Table 6.5.2-3. Base Station Test Model, General
CCDF

- **RC 1/2**
  - 9 channels
  - 64 channels

- **RC 3/4/5**
Reverse signal Setup example

**MS transmitter test**

**BS receiver test**

- **MX368031A**
  - RC 1
  - RC 3
    - FCH + PICH
    - FCH + SCH + PICH
    - DCCH + PICH

- **MX368042A**
  - RC 1
CCDF

- RC 1/2
CCDF

- **RC 3**
  - FCH + PICH
  - FCH + SCH + PICH
  - DCCH + PICH
### Receiver Test

<table>
<thead>
<tr>
<th>Requirements</th>
<th>Meas. Methods</th>
<th>Test</th>
<th>Wanted signal generator</th>
<th>Interfering signal generator</th>
<th>CW generator</th>
<th>BERT</th>
<th>Others</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.4.3.2</td>
<td>7.2.1</td>
<td>Sensitivity</td>
<td>MG3681A +MU368030A +MX368035A</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.4.3.4</td>
<td>7.2.2</td>
<td>Adjacent channel selectivity</td>
<td>MG3681A</td>
<td>MG3642A</td>
<td></td>
<td>MP1201C</td>
<td>MA1612A</td>
</tr>
<tr>
<td>3.4.3.5</td>
<td>7.2.3</td>
<td>Intermodulation characteristics</td>
<td>MG3681A or 3GHz</td>
<td>MG3642A or 2.08GHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.4.3.6</td>
<td>7.2.4</td>
<td>Spurious response</td>
<td>MG3681A</td>
<td>MG3642A</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.4.3.9</td>
<td>7.2.8</td>
<td>Receive signal strength indicator accuracy</td>
<td>MG3681A or 3GHz</td>
<td>MG3642A or 2.08GHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.4.3.10</td>
<td>7.2.9</td>
<td>Bit error rate floor characteristics</td>
<td>MG3681A</td>
<td>MG3642A</td>
<td></td>
<td></td>
<td>MP1201C</td>
</tr>
</tbody>
</table>
Receiver test  Connection example

Interfering signal generator
CW generator
MG3681A
+MU368030A+MX368035A

Wanted signal generator
MG3681A
+MU368030A+MX368035A

CW generator
(MG3642A)

Frame trigger
• Front panel [Trigger] Input
  • 5 ms clock

Controller
• Launches TCH in the receivable state by FTM Factory Test Mode control.

Demodulated (TCH) data
Clock
BERT (MP1201C)

Combiner (MA1612A)
• **Frame trigger delay**
  » Set the timing to which CS can receive Uplink TCH

- Frame trigger
  Input

- Uplink TCH (burst)
  Output
  • In case of outputting TCH (burst) in 5 ms from trigger
    - MG3670 series “Trigger Select: Uplink”

- Uplink TCH (burst)
  Output
  • In case of outputting TCH (burst) in 2.5 ms from trigger
    - MG3670 series “Trigger Select: Downlink”
CS receiver Timing sync. Setup example

- **Setting External Frame trigger**
  - Captures/ Synchronizes the Trigger of 5 ms clock

- **Reference clock:**
  - Apply to cancel the jitter of within ±1/20 symbol of synchronous errors
    - MG3670 series is the jitter within ±1/16 symbol
  - [Ref. Clock] Input applicable case
    - Reference Clock : [Ext(TTL)]
      - $20 \times 192$ kHz (3,840 kHz)
  - [10MHz/13MHz Ref] Input applicable case
    - Reference Clock : [Int]
CS receiver  Timing sync.  Setup example

- **Frame trigger delay**
  - 0 ~ +16,777,215 /20 symbol
  - 1/20 symbol resolution
  - Delay from trigger
    - + 2.55 symbol
    - 2.55 ~ 838,863.3 symbol
  - e.g.
    - In case of outputting TCH (burst) in 5 ms from trigger
      - 19,149 /20 symbol
      - Equivalent to MG3670 series
        - "Trigger Select: Uplink"
          - 19,171 /20 symbol
          - + 0.614 + 0.5 symbol
    - In case of outputting TCH (burst) in 2.5 ms from trigger
      - 9,549 /20 symbol
      - Equivalent to MG3670 series
        - "Trigger Select: Downlink"
          - 9,571 /20 symbol
          - + 0.614 + 0.5 symbol

- **Trigger recapture/synchronization**
Wanted/Interfering signal generator Setup example

- **Wanted signal generator**
  - CS test
    - Uplink
  - PS test
    - Downlink

- **Interfering signal generator**
  - CONPN15
RF/IF components test  Connection example

Signal source
MG3681A
+MU368030A+MX368035A
or
+MU368030A+MX368031A

Reference clock

Signal analyzer (MS8600/MS2680)
Signal Setup example

- **MX368035A**
  - $\pi/4$DQPSK modulation
    - TCH (burst) format
    - Continuous modulation format
  - 16QAM modulation
  - 8PSK modulation
  - QPSK modulation
  - BPSK modulation
    - Continuous modulation format

- **MX368031A**
  - $\pi/4$DQPSK modulation
    - Continuous modulation format
Contrast of typical ACLR

- Burst (TCH) format
  - 600 kHz: +0.5 ~ +1 dB
  - 900 kHz: +1 ~ +2 dB

- Continuous modulation format
# Receiver Test

<table>
<thead>
<tr>
<th>Requirements</th>
<th>Meas Methods</th>
<th>Test</th>
<th>Wanted signal generator</th>
<th>Interfering signal generator</th>
<th>CW generator</th>
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<th>Others</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.4.3.2</td>
<td>6.2.1</td>
<td>Sensitivity</td>
<td>MG3681A + MU368010A + MX368011A</td>
<td>MG3681A + MU368010A + MX368011A</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>3.4.3.4</td>
<td>6.2.2</td>
<td>Adjacent channel selectivity</td>
<td>MG3681A + MU368010A + MX368011A</td>
<td>MG3681A + MU368010A + MX368011A</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>3.4.3.5</td>
<td>6.2.3</td>
<td>Intermodulation characteristics</td>
<td>MG3681A + MU368010A + MX368011A</td>
<td>MG3681A + MU368010A + MX368011A</td>
<td>-</td>
<td>-</td>
<td>-</td>
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<tr>
<td>3.4.3.6</td>
<td>6.2.4</td>
<td>Spurious response</td>
<td>MG3681A + MU368010A + MX368011A</td>
<td>MG3681A + MU368010A + MX368011A</td>
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<td>-</td>
<td>-</td>
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<tr>
<td>3.4.3.8</td>
<td>6.2.6</td>
<td>Interference level (CIR)</td>
<td>MG3681A + MU368010A + MX368011A</td>
<td>MG3681A + MU368010A + MX368011A</td>
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<td>-</td>
<td>-</td>
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<tr>
<td>3.4.3.10</td>
<td>6.2.8</td>
<td>Reception level detection</td>
<td>MG3681A + MU368010A + MX368011A</td>
<td>MG3681A + MU368010A + MX368011A</td>
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<tr>
<td>3.4.3.11</td>
<td>6.2.9</td>
<td>Network quality detection accuracy</td>
<td>MG3681A + MU368010A + MX368011A</td>
<td>MG3681A + MU368010A + MX368011A</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>
Receiver test  Connection example

Interfering signal generator
CW generator
MG3681A
+MU368010A+MX368011A

Wanted signal generator
MG3681A
+MU368010A+MX368011A

CW generator
(MG3642A)

– Frame trigger
  • Front panel [Burst Trig] Input
    – 20 ms clock (Full rate), 40 ms clock (Half rate)

– Controller
  • Launches TCH in the receivable state by FTM Factory Test Mode control.
BS receiver  Timing sync.  Setup example

- Setting External Frame trigger
  - Captures/ Synchronizes the Trigger of 20 ms clock (Full rate)/ 40 ms clock (Half rate)

- [10MHz/13MHz Ref] Input:
  - Apply to cancel the jitter of within ±1/16 symbol of synchronous errors
  - MG3670 series is the jitter within ±1/16 symbol
Scramble pattern sync. Setup example

- Scramble pattern
  - PN(9,5)
    - Register initial data ($S_8 \sim S_0$) = CC
Wanted/Interfering signal generator Setup example

- **Wanted signal generator**
  - BS test
    - UP TCH
  - MS test
    - DN TCH ALL

- **Interfering signal generator**
Packet communication Receiver test Setup example

- **Wanted signal generator**
  MG3681A
  + MU368030A + MX368034A
  » BS test
    Uplink UPCH
    - UP1
  » MS test
    Downlink UPCH
    - DN1
    - DN2
    - DN3
• **Frame trigger delay**
  » Set the timing to which BS can receive Uplink UPCH

- Frame trigger input
- Uplink UPCH (burst) output
  - Outputting UPCH (burst) in 20 ms from trigger

20 ms (420 symbol)

6.66 ms (140 symbol)
BS receiver  Timing sync.  Setup example

- **Setting External Frame trigger**
  » Captures/ Synchronizes the Trigger of 20 ms clock

- **Reference clock:**
  Apply to cancel the jitter of within ±1/16 symbol of synchronous errors
  » [Ref. Clock] Input applicable case
    - Reference Clock: [Ext(TTL)]
      • $16 \times 21$ kHz (336 kHz)
  » [10MHz/13MHz Ref] Input applicable case
    - Reference Clock: [Int]

- **Frame trigger delay**
  » $0 \sim +16,777,215 /16$ symbol
    1/16 symbol resolution
  » Delay from trigger
    + 3.7 symbol
    - $3.7 \sim 1,048,579.6$ symbol

- **Trigger recapture/ synchronization**
  e.g.
  » In case of outputting UPCH (burst) in 20 ms from trigger
    • $6,661 /16$ symbol
RF/IF components test

**Connection example**

Signal source
MG3681A
+MU368010A+MX368011A
or
+MU368030A+MX368031A

Reference clock

Signal analyzer
( MS8600/MS2680 )
Signal Setup example

- **MX368011A**
  - Burst format
  - Continuous modulation format

- **MX368031A**
  - Continuous modulation format
Contrast of typical ACLR

- Burst (TCH) format
  - 50 kHz: +7 dB
  - 100 kHz: +7 dB

- Continuous modulation format
Signal source
MG3681A
+MU368030A+MX368031A

Reference clock

Signal analyzer
(MS8600/MS2680)
Signal Setup example

- Continuous modulation format
Option

- MG3681A-01, 02
  » Reference oscillator
- MG3681A-11
  » Additional function of I/Q output
- MG3681A-21
  » AF synthesizer
- MG3681A-42
  » RF high level output
- MA2512A
  » Band Pass Filter
MG3681A-01, 02  Reference oscillator

- Exchangeable to long-term stable internal reference oscillator

<table>
<thead>
<tr>
<th></th>
<th>Standard</th>
<th>MG3681A-01</th>
<th>MG3681A-02</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aging rate</td>
<td>±1 x 10^-6/year</td>
<td>±5 x 10^-9/day</td>
<td>±5 x 10^-10/day</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(±5 x 10^-8/year)</td>
<td>(±2 x 10^-8/year)</td>
</tr>
<tr>
<td>Warm-up stability</td>
<td>±1 x 10^-7</td>
<td>±1 x 10^-7</td>
<td></td>
</tr>
<tr>
<td>Temperature stability (0 ~ 50 °C)</td>
<td>±1 x 10^-6</td>
<td>±3 x 10^-8</td>
<td>±5 x 10^-9</td>
</tr>
</tbody>
</table>

* Warm-up stability: After 10 minute (compared to frequency after 24 hours)

- Frequency accuracy is specified by the aging rate of reference oscillator.
  
  » Frequency accuracy
  
  \[ \text{Frequency accuracy} = \pm \text{Output frequency} \times \text{Aging rate} \times \text{Time since last calibrated} \]

  e.g.

  \[ \text{2 GHz} \times 2 \times 1 \text{ year} = \pm 2 \text{ kHz} \]

  * Standard

  \[ \text{2 GHz} \times 40 \times 1 \text{ year} = \pm 40 \text{ Hz} \]

  * MG3681A-02
Warm-up stability

• The long-term stable internal reference oscillator of MG3681A-01 and 02 uses OCXO of the oven system which stabilizes frequency only 10 minutes after the main power ON.
  » Since oven is preheated in power standby state, frequency is stabilized immediately after power ON from only 10 minutes standby state.
• Standard internal reference oscillator uses TCXO with unnecessary preheating.
Effect of frequency accuracy on receiver sensitivity test

- In case of more frequency uncertainty (poor frequency accuracy), receiver is tested as deteriorated sensitivity than true value.
  - The level of the signal is lost when the received signal is located in the skirt of BPF in a receiver by frequency uncertainty.
MG3681A-11  Additional function of I/Q output

• Variable of voltage level of I/Q signals output, DC offset and quadrature degree
  » Voltage level: 80 ~ 120 % resolution 0.1 %
    - RMS level ($\sqrt{I^2+Q^2}$) is specified in each system software.
  » DC offset: -0.5 ~ +1.5 V resolution 0.5 mV
  » Quadrature degree: -5 ~ +5 ° resolution 0.5 °

• Differential I/Q signals can be outputted.
  » $\bar{I}/\bar{Q}$ signals which are reversal signals (amplitude is equal and polarity is reverse) of I/Q signals are outputted.
Variable application of voltage level of I/Q signals output, DC offset and quadrature degree

- In order to test the vector modulator, the setup of vector magnitude, drive DC voltage and I/Q quadrature degree is required for the signal source.
  - **Vector Magnitude**
    - Voltage level is set as RMS level of the vector modulator.
  - **Drive DC voltage**
    - In order to drive the vector modulator of the single power supply system, DC offset is set as drive voltage.
  - **Quadrature degree**
    - In order to cancel the error of I/Q quadrature degree (90°) of the vector modulator, quadrature degree is set.
Variable of voltage level of I/Q signals output, DC offset and quadrature degree

- Setup example
  - Voltage level
    - Specified 141 mV(rms)
    → 150 mV(rms) ≈ 106%
  - DC offset
    - +1 V
  - Quadrature degree
    - Fine tuning

\[ \sqrt{I^2 + Q^2} = 150 \text{ mV} \]
\[ \sqrt{I^2 + Q^2} = 141 \text{ mV} \]
Application of differential I/Q signals

• In order to test the vector modulator and baseband LSI for balanced device, the output of I, I, Q and Q balance is required for the signal source.

• In I/Q input device, the balanced input has the advantage which can reduce the amplitude error and the noise compared with I and Q unbalanced input (single end).
  » Reduction of the amplitude error by the grand loop
    – The cause is that the ground of the signal source and the ground of the input device are not equivalent potential.
  » Reduction of a signal line noise
    – The cause is that the environmental noise is picked up on the signal line.

• For outputting differential I/Q signals
  » I/Q Output: [On]
MG3681A-21  AF synthesizer

- AF can be outputted.

  » 0.01 Hz ~ 400 kHz
  » resolution 0.01 Hz
  Sine wave  Triangle wave
  Square wave  Sawtooth wave
MG3681A-21  AF synthesizer

• Internal analog modulation signal can be outputted.

  » AM
    \[ V_{AM}(t) = A_c [1 + m s(t)] \cos(2\pi f_c t) \]
    • \( m \): Modulation index (Modulation depth)

  » FM
    \[ V_{FM}(t) = A_c \cos[2\pi f_c t + m \int s(t)dt] \]
    • \( m \): Frequency modulation index (Frequency deviation)

  » \( \phi \)M (PM)
    \[ V_{PM}(t) = A_c \cos[2\pi f_c t + m s(t)] \]
    • \( m \): Phase modulation index (Phase deviation)

• \( A_c \): Carrier amplitude
• \( s(t) \): Modulation signal (AF)
• \( f_c \): Carrier frequency (RF)
External analog modulation

- Input Modulation signal (AF).

- Wideband AM
  - Applicable to wideband (high-speed) video modulation
  - ASK modulation is achieved by AM.
    - Modulation signal
    - ASK
RF output level range in CDMA modulation signals can be gained 8 dB without degrading the adjacent channel leakage power ratio.

- at outputting 1.9 to 2.3 GHz used as the frequency band for IMT-2000 systems
- ACLR does not degrade up to +5 dBm in W-CDMA/CDMA2000 modulation.
Application

• Useful for signal source of power amplifier requiring a high input level
Typ. ACLR

- **W-CDMA**
  - Test Model 1: 16 DPCH

![Graph showing ACLR (5MHz) vs. Output level [dBm]](image)
Maximum output level  (1.9~2.3 GHz)

<table>
<thead>
<tr>
<th></th>
<th>Standard</th>
<th>MG3681A-42</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>W-CDMA modulation</strong></td>
<td></td>
<td>+8 dB gain</td>
</tr>
<tr>
<td>Number of multiplex channel: dBm</td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td></td>
<td>+5</td>
<td>+13</td>
</tr>
<tr>
<td>» 1~7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>» 8~12</td>
<td>+4</td>
<td>+12</td>
</tr>
<tr>
<td>» 13~15</td>
<td>+3</td>
<td>+11</td>
</tr>
<tr>
<td>» 16~19</td>
<td>+2.14</td>
<td>+10.14</td>
</tr>
<tr>
<td>» 20~31</td>
<td>+2</td>
<td>+10</td>
</tr>
<tr>
<td>» 32~50</td>
<td>+1</td>
<td>+9</td>
</tr>
<tr>
<td>» 51~</td>
<td>0</td>
<td>+8</td>
</tr>
<tr>
<td><strong>CDMA2000 modulation</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>»</td>
<td>+5</td>
<td>+13</td>
</tr>
<tr>
<td><strong>CW</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>»</td>
<td>+17 Typ. +19 (Setting: +25)</td>
<td></td>
</tr>
</tbody>
</table>
Typ. output level frequency response

- Level +5 dBm setting (CW)
MA2512A Band Pass Filter

- The unnecessary spurious signal of a signal generator can be attenuated.
  - at outputting 1.92 to 2.17 GHz used as the frequency band for IMT-2000 systems
  - Excellent amplitude ripple and group delay characteristics don’t degrade modulation accuracy of the signal.
Application

• When spurious signals hinder components evaluation
  » Spurious signals of MG3681A
     – 660 MHz (IF leakage)
     – +660 MHz offset (Local leakage)
     – 2×frequency/3×frequency (2nd/3rd harmonics)

Signal source
MG3681A
+MU368040A+MX368041B

Reference clock

Signal analyzer
(MS8600/MS2680)
Improvement of spurious

\[ f_{LO} \leq f_{c} \leq -80 \text{ dBc} \]
Loss frequency response

Pass band
• 1.92~2.17 GHz (IMT-2000 system band)
• Insertion loss \( \leq 3.5 \text{ dB} \)
• Return loss \( \geq 15 \text{ dB} \)

Filter band
• DC ~ 1.5 G, 2.58 ~ 7 GHz
• Attenuation \( \geq 20 \text{ dB} (< 5 \text{ GHz}) \)
  \( \geq 10 \text{ dB} (\geq 5 \text{ GHz}) \)
Modulation accuracy not degrading

- Amplitude ripple
  \[ \leq 0.2 \text{ dB} \] (5 MHzBW)

- Group delay
  \[ \leq 1 \text{ ns} \] (5 MHzBW)